Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM25Q128

128M-BIT SERIAL FLASH MEMORY

Datasheet

May. 2019

Trademarks

1. Description

The FM25Q128 is a 128M-bit (16,384K-byte) Serial Flash memory, with advanced write protection mechanisms. The FM25Q128 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O as well as 2-clock instruction cycle Quad Peripheral Interface (QPI).

The FM25Q128 can be programmed 1 to 256 bytes at a time, using the Page Program instruction. It is designed to allow either single Sector/Block at a time or full chip erase operation. The FM25Q128 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

2. Features

- **128Mbit of Flash memory**
  - 4096 uniform sectors with 4K-byte each
  - 256 uniform blocks with 64K-byte each or
  - 512 uniform blocks with 32K-byte each
  - 256 bytes per programmable page
- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - QPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - Continuous READ mode support
  - Allow true XIP (execute in place) operation
- **High Performance**
  - 104MHz Standard/Dual/Quad SDR SPI clocks
  - 208/416MHz equivalent Dual/Quad SPI
  - Endurance: 100,000 program/erase cycles
  - Data retention: 20 years
- **Supply Voltage: 2.7V to 3.6V**
- **Industrial Temperature Rage**
- **Flexible Architecture with 4KB Sectors**
  - Uniform Sector Erase(4K-bytes)
  - Uniform Block Erase(32K and 64K-bytes)
  - Program 1 to 256 bytes per programmable page
- **Advanced Security Features**
  - Software and hardware write protection
  - Top/Bottom, 4KB complement array protection
  - Power Supply Lock-Down
  - Advanced Sector protection
  - Extra 2X512-Byte Register
  - Discoverable Parameters (SFDP) Register
  - 64-Bit Unique ID for each device
  - Volatile & Non-volatile Status Register Bits
- **Green Package**
  - 8-pin SOP (208mil)
  - 8-pin TDFN (8x6mm)
  - 8-pin TDFN (5x6mm)
  - All Packages are RoHS Compliant and Halogen-free

3. Packaging Type and Pin Configurations

FM25Q128 is offered in an 8-pin SOP (208mil) and an 8-pin TDFN (8x6mm) and an 8-pin TDFN (5x6mm) packages as shown in Figure 1-3 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1. Pin Configuration 8-Pin SOP (208mil)

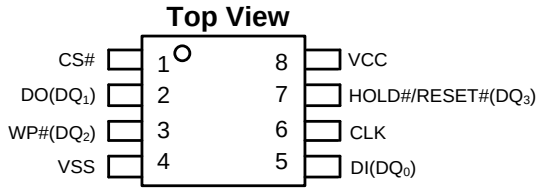


Figure 1 FM25Q128 pin assignments, 8-pin SOP (208mil)

3.2. Pin Configuration 8-Pin TDFN (8x6mm)

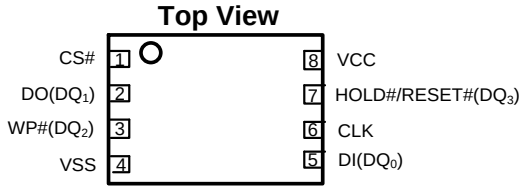


Figure 2 FM25Q128 pin assignments, 8-pin TDFN (8x6mm)

3.3. Pin Configuration 8-Pin TDFN (5x6mm)

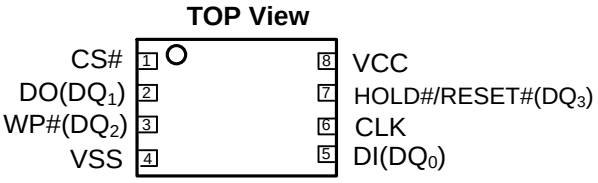


Figure 3 FM25Q128 pin assignments, 8-pin TDFN (5x6mm)

3.4. Pin Description SOP8 (208mil), TDFN8 (8x6mm) , TDFN8 (5x6mm)

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ_1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ_2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (DQ_0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD#/RESEST# (DQ_3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Note:
1 DQ_0 and DQ_1 are used for Dual SPI instructions.
2 DQ_0 – DQ_3 are used for Quad SPI and QPI instructions

4. PIN DESCRIPTIONS

4.1. Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up (see “8 Write Protection” and Figure 75). If needed a pull-up resister on CS# can be used to accomplish this.

4.2. Serial Data Input, Output and I/Os (DI, DO and DQ0, DQ1, DQ2, DQ3)

The FM25Q128 supports standard SPI, Dual SPI, Quad SPI and QPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual/Quad SPI and QPI instructions use the bidirectional DQ pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the WP# pin becomes DQ_2 and HOLD# pin becomes DQ_3.

4.3. Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. Used in conjunction with the Status Register’s Block Protect (CMP, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The WP# pin is active low. However, when the QE bit of Status Register-2 is set for Quad I/O, the WP# pin function is not available since this pin is used for DQ2.

4.4. HOLD (HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When HOLD**#** is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, and the HOLD/RST bit of Status Register-3 is cleared, the HOLD# pin function is not available since this pin is used for DQ_3.

4.5. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

4.6. Reset (RESET#)

The RESET# pin allows the device to be reset by the controller. For 8-pin packages, when the HOLD/RST bit of Status Register-3 is set, the IO3 pin acts as RESET# function in despite of QE bit setting.

5. Block Diagram

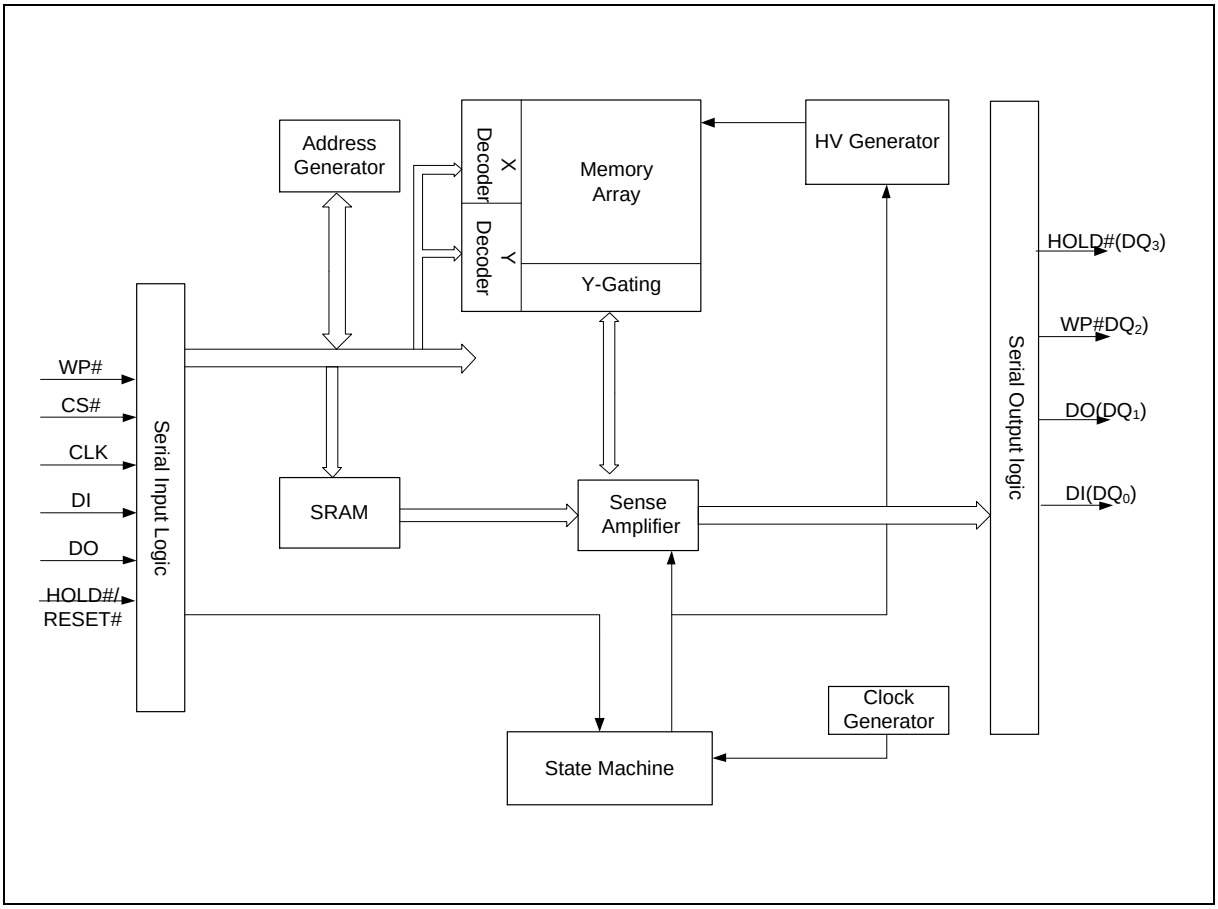


Figure 4 FM25Q128 Serial Flash Memory Block Diagram

6. Memory Organization

The FM25Q128 array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed (bits are programmed from 1 to 0) at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The FM25Q128 has 4,096 erasable sectors, 512 erasable 32-k byte blocks and 256 erasable 64-k byte blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

Table 1 Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
255	511 | 510	4095	FFF000h	FFFFFFh
		…	…	…
		4080	FF0000h	FF0FFFh
.....	.....	.....	.....	.....
		.....	.....	.....
		.....	.....	.....
248	497 | 496	3983	F8F000h	F8FFFFh
		…	…	…
		3968	F80000h	F80FFFh
.....	.....	.....	.....	.....
		.....	.....	.....
		.....	.....	.....
15	31 | 30	255	0FF000h	0FFFFFh
		…	…	…
		240	0F0000h	0F0FFFh
.....	.....	.....	.....	.....
		.....	.....	.....
		.....	.....	.....
8	17 | 16	143	08F000h	08FFFFh
		…	…	…
		128	080000h	080FFFh
7	15 | 14	127	07F000h	07FFFFh
		…	…	…
		112	070000h	070FFFh
.....	.....	.....	.....	.....
		.....	.....	.....
		.....	.....	.....
2	5 | 4	47	02F000h	02FFFFh
		…	…	…
		32	020000h	020FFFh
1	3 | 2	31	01F000h	01FFFFh
		…	…	…
		16	010000h	010FFFh
0	1 | 0	15	00F000h	00FFFFh
		…	…	…
		2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

7. Device Operations

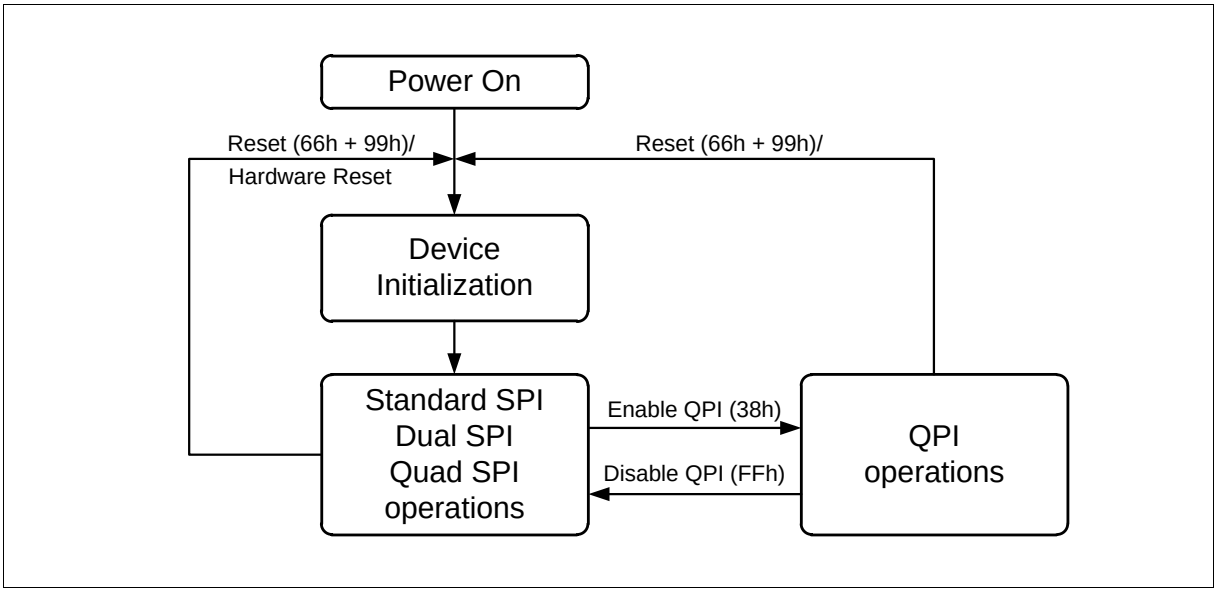


Figure 5 FM25Q128 Serial Flash Memory Operation Diagram

7.1. Standard SPI

The FM25Q128 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device. The DO output pin is used to read data or status from the device.

Commands, write instructions, addresses or data are latched on the rising edge of CLK, read data or status are available on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

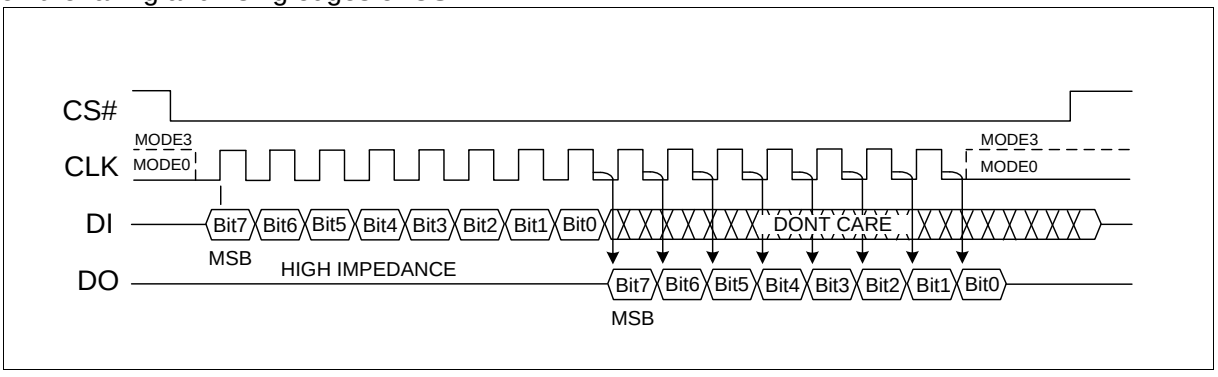


Figure 6 The difference between Mode 0 and Mode 3

7.2. Dual SPI

The FM25Q128 supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” , “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

7.3. Quad SPI

The FM25Q128 supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “Word Read Quad I/O (E7h)”, “Octal Word Read Quad I/O (E3h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.4. QPI

The FM25Q128 supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four DQ pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enable QPI (38h)” and “Disable QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction or hardware reset, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively. See Figure 5 for the device operation modes.

7.5. Hold

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25Q128 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

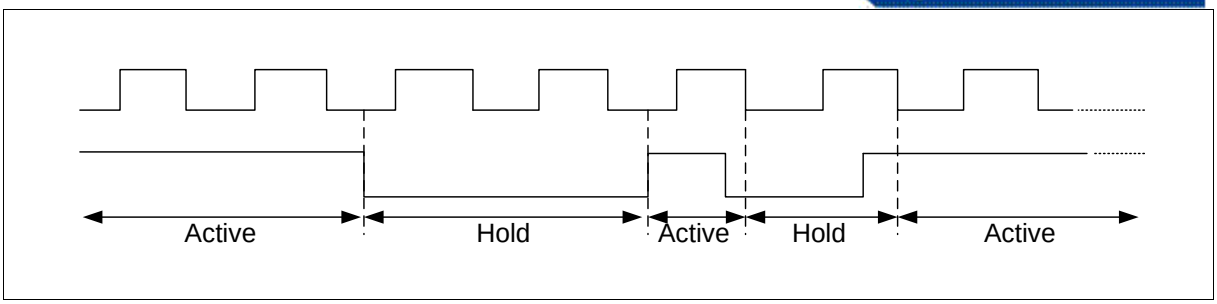


Figure 7 Hold Condition Waveform

7.6. Software Reset & Hardware Reset

The FM25Q128 can be reset to the initial power-on state by a Software Reset sequence, either in SPI or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the commands sequence is successfully accepted, the device will take t_{RHSL} to reset. No command will be accepted during the reset period.

For the SOP8 and TDFN8 package types, FM25Q128 can also be configured to utilize a hardware RESET# pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for HOLD# pin function or RESET# pin function. When HOLD/RST=0 (factory default), the pin acts as a HOLD# pin as described above; when HOLD/RST=1, the pin acts as a RESET# pin. Drive the RESET# pin low for a minimum period of ~1us (t_{RLRH}) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While RESET# is low, the device will not accept any command input.

If QE bit is set to 1, the HOLD# or RESET# function will be disabled, the pin will become one of the four data I/O pins.

Drive the RESET# pin low for a minimum period of ~1us (t_{RLRH}) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated RESET# pin.

Hardware RESET# pin has the highest priority among all the input signals. Drive RESET# low for a minimum period of ~1us (t_{RLRH}) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (CS#, CLK, DI, DO, WP# and/or HOLD#).

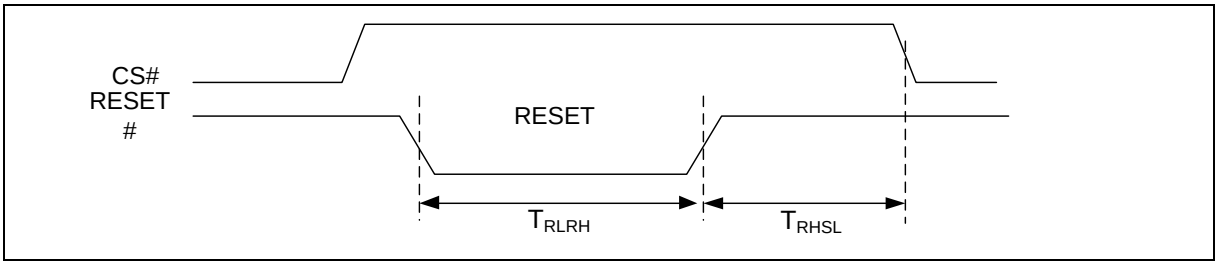


Figure 8 Hardware RESET Condition

Note:
1. While a faster RESET# pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum time is recommended to ensure reliable operation.
2. **Data corruption may happen if there is an on-going when software reset or hardware reset is accepted by the device.** It is recommended to check the WIP bit in Status Register before issuing the software reset command or hardware reset.

8. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25Q128 provides several means to protect the data from inadvertent writes.

Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Advanced Sector Protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up

At power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on VCC until VCC reaches the correct values: V_{CC}(min) at power-up and VSS at power-down.

To avoid data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while VCC is less than the power-on reset threshold voltage of V_{CC} (low); all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands. After power-up, the device is in standby power mode.

In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

At power-down, when VCC drops from the operating voltage to below the threshold voltage V_{CC}(low), all operations are disabled and the device does not respond to any command.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may result.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion as small as a 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The FM25Q128 also provides another Write Protect method using the individual Block Locks. Each 64KB block(except the top and bottom blocks, total of 254 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with a Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An “Individual Block Unlock(39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0(factory default), the device will only utilize CMP, TB, BP[2:0] to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks and CMP, TB, BP[2:0] for write protection, each protect scheme for the corresponding is available.

9. Status Register

Three Status Registers are provided for FM25Q128. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the Flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Sector lock status, and output driver strength. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Hold/RESET functions and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP), the Write Enable instruction, and during Standard/Dual SPI operations, the WP# pin.

Factory default for all Status Register bits are 0.

9.1. Status Register-1(SR1)

Related Commands: Read Status Register (RDSR1 05h), Write Status Register (WRSR 01h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register (50h).

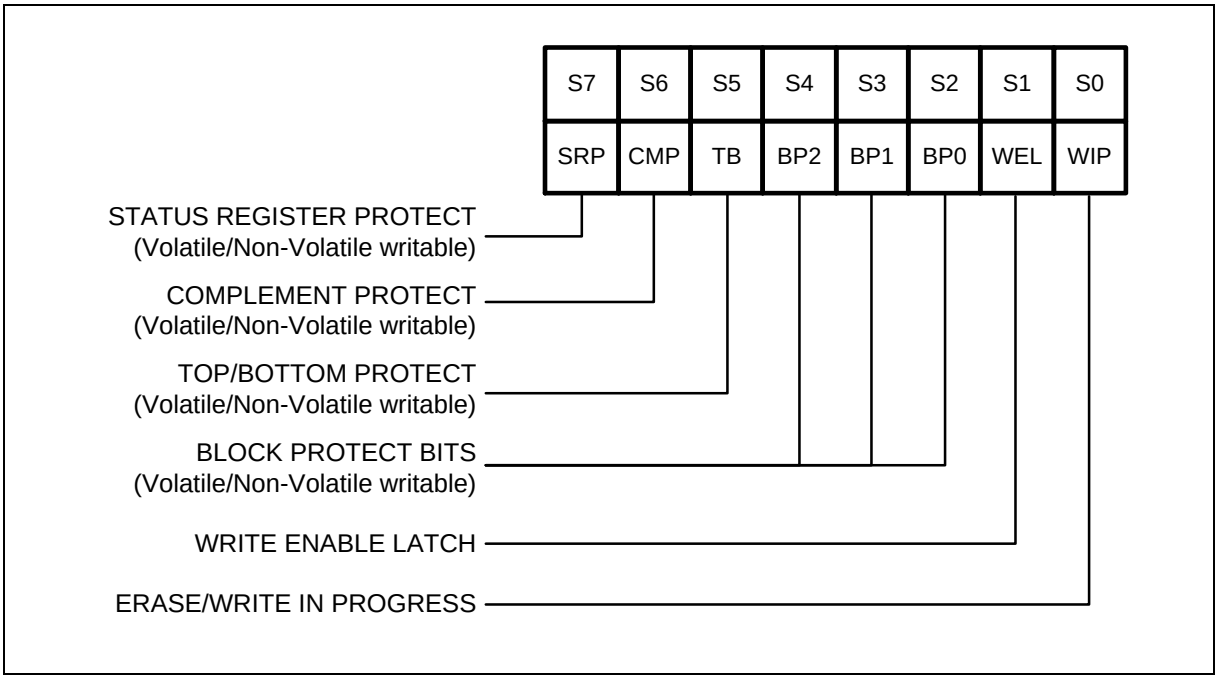


Figure 9 Status Register-1

9.1.1. Write In Progress (WIP)

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Sector instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see tW, tPP, tSE, tBE, and tCE in “11.6 AC Electrical Characteristics”). When the program, erase or write status register (or security sector) instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.1.2. Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Sector and Program Security Sector.

9.1.3. Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in "11.6 AC Electrical Characteristics"). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

9.1.4. Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP and WEL bits.

9.1.5. Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S6). It is used in conjunction with TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to Status Register Memory Protection table for details. The default setting is CMP=0.

9.1.6. Status Register Protect (SRP)

The Status Register Protect bit (SRP) is non-volatile read/write bit in the status register (S7). The SRP bit controls the method of write protection: software protection, hardware protection.

Table 2 Status Register Protect bit

SRP	WP#	Status Register	Description
0	X	Software Protection	WP# pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. (Factory Default)
1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
1	1	Hardware Unprotected	When WP# pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.

9.2. Status Register-2 (SR2)

Related Commands: Read Status Register-2 (RDSR2 35h), Write Status Register-2 (WRSR2 31h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register (50h).

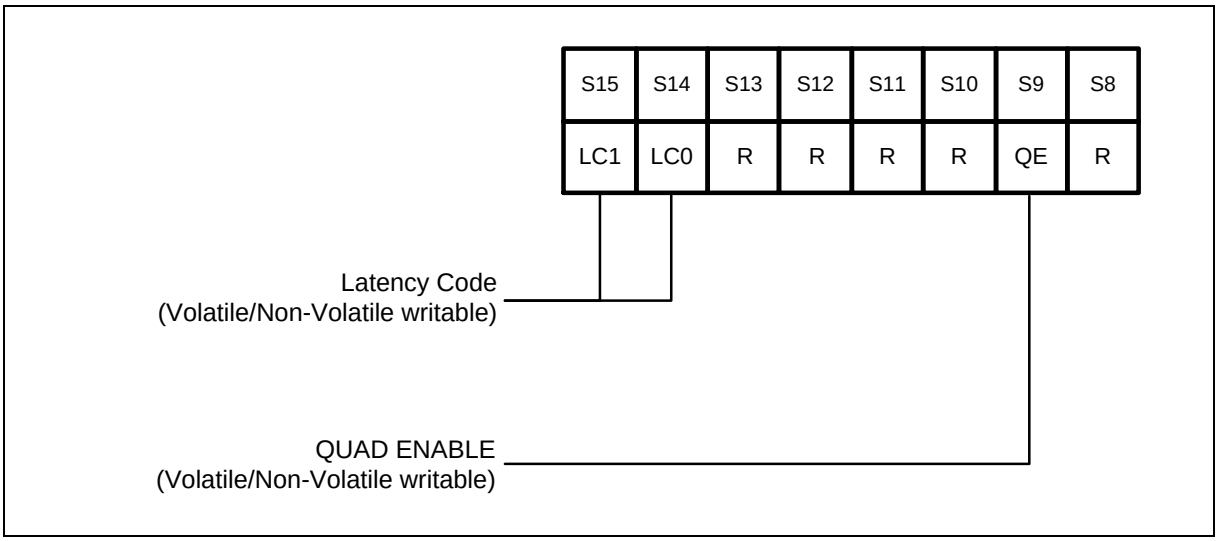


Figure 10 Status Register-2

9.2.1. Latency Code (LC1, LC0)

The Latency Code bits (LC1 and LC0) are non-volatile read/write bits in the status register (S15 and S14). The Latency Code selects the number of continuous mode and dummy cycles between the end of address and the start of read data output for all read commands.

Table 3 Latency Code bits for SPI mode

LC	Fast Read		Read Dual Out		Read Quad Out		Dual I/O Read		Quad I/O Read		Word Read Quad I/O		Octal Word Read Quad I/O	
	0Bh		3Bh		6Bh		BBh		EBh		E7h		E3h	
	mode	dummy	mode	dummy	mode	dummy	mode	dummy	mode	dummy	mode	dummy	mode	dummy
00	0	8	0	8	0	8	4	0	2	4	2	2	2	0
01	0	8	0	8	0	8	4	4	2	6	2	4	2	2
10	0	8	0	8	0	8	4	4	2	8	2	6	2	4
11	0	0	0	0	0	8	4	0	2	2	2	2	2	0

Table 4 Latency Code bits for QPI mode

Freq. (MHz)	LC	Fast Read		Quad I/O Read		QPI wrap read	
		0Bh		EBh		0Ch	
		mode	dummy	mode	dummy	mode	dummy
≤80	00	0	6	2	4	0	6
≤104	01	0	8	2	6	0	8
≤104	10	0	10	2	8	0	10
≤50	11	0	4	2	2	0	4

9.2.2. Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to 1, and the HOLD/RST bit of Status Register-3 is cleared, the Quad DQ2 and DQ3 pins are enabled, and WP# and HOLD# functions are

disabled.

QE bit is required to be set to a 1 before issuing an “Enable QPI (38h)” to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A “Write Status Register” command in QPI mode cannot change QE bit from a “1” to a “0”.

WARNING: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

9.3. Status Register-3 (SR3)

Related Commands: Read Status Register-3 (RDSR3 15h), Write Status Register-3 (WRSR3 11h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register (50h). Write Enable (WREN 06h) can be used to clear P-Fail/E-Fail bit of SR3 if P-Fail/E-Fail is set to 1 by the last operation.

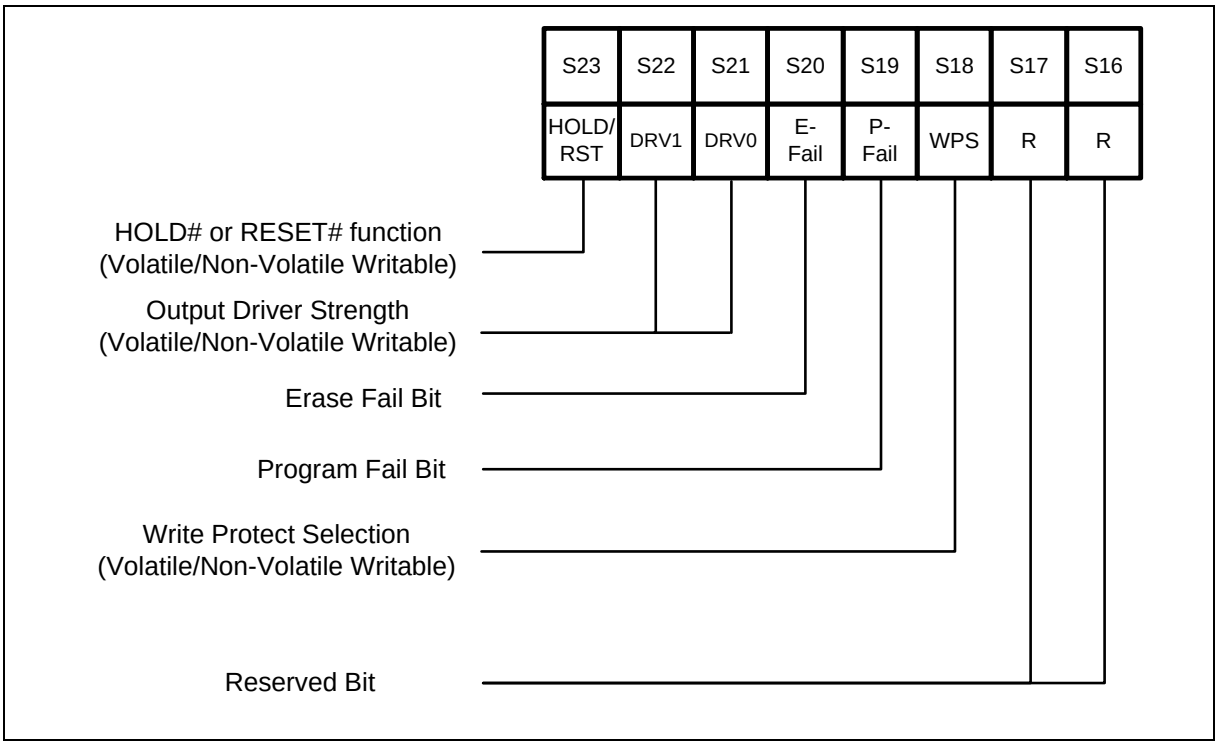


Figure 11 Status Register-3

9.3.1. HOLD# or RESET# pin function (HOLD/RST)

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as HOLD#; when HOLD/RST=1, the pin acts as RESET# in despite of QE bit setting. If QE is set to 1, the HOLD# function is disabled, the pin acts as a dedicated data I/O pin.

9.3.2. Write Protect Selection (WPS)

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, BP[2:0] to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

9.3.3. Output driver strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength.

Table 5 Driver strength configuration

DRV1, DRV0	Driver Strength
0,0	100%
0,1	75%
1,0	50%
1,1	25%

9.3.4. Program Fail Bit (P-Fail)

The Program Fail bit is a status flag, which shows the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected.

9.3.5. Erase Fail Bit (E -Fail)

The Erase Fail bit is a status flag, which shows the status of last Erase operation. It will be set to "1", if the Erase operation fails or the Erase region is protected.

9.4. Status Register Memory Protection (WPS=0, CMP=0)

Table 6 Status Register Memory Protection (WPS=0, CMP=0)

STATUS REGISTER					FM25Q128 (128M-BIT) MEMORY PROTECTION			
CMP	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h – FFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h – FFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h – FFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h – FFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h – FFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h – FFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h – 0FFFFFh	1M	Lower 1/16
0	1	1	0	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h –	4MB	Lower 1/4

STATUS REGISTER					FM25Q128 (128M-BIT) MEMORY PROTECTION			
CMP	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
						3FFFFFh		
0	1	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
0	X	1	1	1	0 thru 255	000000h – FFFFFFh	16MB	ALL

9.5. Status Register Memory Protection (WPS=0, CMP=1)

Table 7 Status Register Memory Protection (WPS=0, CMP=1)

STATUS REGISTER					FM25Q128 (128M-BIT) MEMORY PROTECTION			
CMP	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
1	X	0	0	0	0 thru 255	000000h – FFFFFFh	16MB	ALL
1	0	0	0	1	0 thru 251	000000h – FBFFFFh	16,128KB	Lower 63/64
1	0	0	1	0	0 thru 247	000000h – F7FFFFh	15,872KB	Lower 31/32
1	0	0	1	1	0 thru 239	000000h – EFFFFFh	15MB	Lower 15/16
1	0	1	0	0	0 thru 223	000000h – DFFFFFh	14MB	Lower 7/8
1	0	1	0	1	0 thru 191	000000h – BFFFFFh	12MB	Lower 3/4
1	0	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
1	1	0	0	1	4 thru 255	040000h – FFFFFFh	16,128KB	Upper 63/64
1	1	0	1	0	8 thru 255	080000h – FFFFFFh	15,872KB	Upper 31/32
1	1	0	1	1	16 thru 255	100000h – FFFFFFh	15MB	Upper 15/16
1	1	1	0	0	32 thru 255	200000h – FFFFFFh	14MB	Upper 7/8
1	1	1	0	1	64 thru 255	400000h – FFFFFFh	12MB	Upper 3/4
1	1	1	1	0	128 thru 255	800000h – FFFFFFh	8MB	Upper 1/2
1	X	1	1	1	NONE	NONE	NONE	NONE

9.6. Status Register Memory Protection (WPS=1)

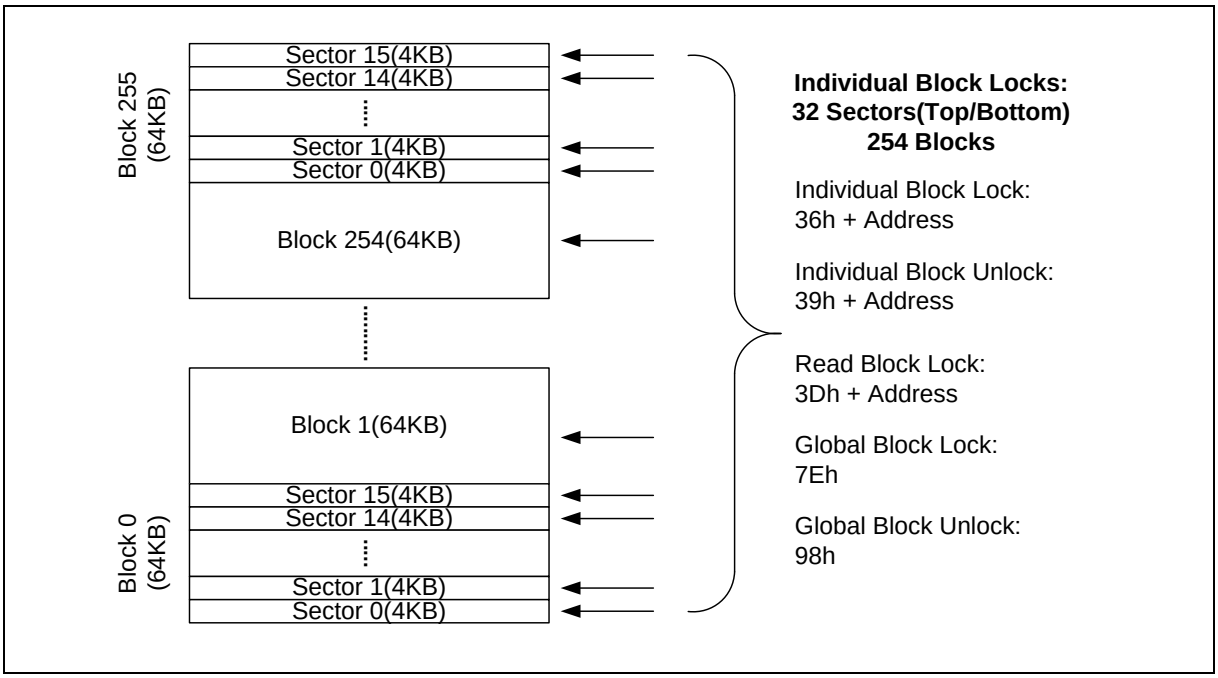


Figure 12 Individual Block/Sector Locks

10. Instructions

The Standard/Dual/Quad SPI instruction set of the FM25Q128 consists of 43 basic instructions that are fully controlled through the SPI bus (see Table 9~ Table 11 Instruction Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the FM25Q128 consists of 29 basic instructions that are fully controlled through the SPI bus (see Table 12 Instruction Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked through DQ[3:0] pins provides the instruction code. Data on all four DQ pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four DQ pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of CS#. Clock relative timing diagrams for each instruction are included in Figure 13 through Figure 74. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.1. Device ID and Instruction Set Tables

10.1.1. Manufacture and Device Identification

Table 8 Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-ID0
ABh			17h
90h, 92h, 94h	A1h		17h
9Fh	A1h	4018h	

10.1.2. Standard SPI Instructions Set

Table 9 Standard SPI Instructions Set (1)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)(2)				
Write Status Register-1(3)	**01h**	(S7-S0) (3)				
Read Status Register-2	**35h**	(S15-S8)(2)				
Write Status Register-2	**31h**	(S15-S8)				
Read Status Register-3	**15h**	(S23-				

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
		S16)(2)				
Write Status Register-3	**11h**	(S23-S16)				
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(4)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Power-down	**B9h**					
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Release Powerdown / ID(5)	**ABh**	dummy	dummy	Dummy	(ID7-ID0)(2)	
Manufacturer/Device ID(5)(6)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID(6)	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read SFDP Register	**5Ah**	00h	00h	A7-A0	dummy	(D7-D0)
Read Unique ID(6)	**4Bh**	dummy	dummy	dummy	dummy	(UID63-UID0)
Erase Security Sectors(7)	**44h**	A23-A16	A15-A8	A7-A0		
Program Security Sectors(7)	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0
Read Security Sectors(7)	**48h**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Enable QPI	**38h**					
Enable Reset	**66h**					
Reset	**99h**					
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0		
Global Block Lock	**7Eh**	A23-A16	A15-A8	A7-A0		
Global Block Unlock	**98h**	A23-A16	A15-A8	A7-A0		

10.1.3. Dual SPI Instructions Set

Table 10 Dual SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0, …)(9)
Fast Read Dual I/O	**BBh**	A23-A8(8)	A7-A0, M7-M0(8)	Dummy(15)	(D7-D0, …)(9)	
Manufacturer/Device ID by Dual I/O(5)(6)	**92h**	A23-A8(8)	A7-A0, M7-M0(8)	(MF7-MF0, ID7-ID0)		

10.1.4. Quad SPI Instructions Set

Table 11 Quad SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Quad Page Program	**32h**	A23-A16	A15-A8	A7-A0	D7-D0, …(11)	D7-D0, …(11)
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy(18)	(D7-D0, …)(11)
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0(10)	Dummy(15)	(D7-D0, …)(11)		
Word Read Quad I/O(12)	**E7h**	A23-A0, M7-M0(10)	Dummy(15)	(D7-D0, …)(11)		
Octal Word Read Quad I/O(13)	**E3h**	A23-A0, M7-M0(10)	Dummy(15)	(D7-D0, …)(11)		
Set Burst with Wrap	**77h**	xxxxx, W6-W4(10)				
Manufacture/Device ID by Quad I/O(5)(6)	**94h**	A23-A0, M7-M0(10)	xxxx, (MF7-MF0, ID7-ID0)	(MF7-MF0, ID7-ID0, …)		

10.1.5. QPI Instructions Set

Table 12 QPI Instructions Set (14)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0,1)*	*(2,3)*	*(4,5)*	*(6,7)*	*(8,9)*	*(10,11)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)(2)				
Write Status Register-1(3)	**01h**	(S7-S0)(3)				
Read Status Register-2	**35h**	(S15-S8)(2)				
Write Status Register-2	**31h**	(S15-S8)				
Read Status Register-3	**15h**	(S23-S16)(2)				
Write Status Register-3	**11h**	(S23-S16)				
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0(11)	D7-D0(4)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Power-down	**B9h**					
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy(15)	(D7-D0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0(15)	(D7-D0)
Release Powerdown / ID(5)	**ABh**	dummy	dummy	dummy	(ID7-ID0)(2)	
Manufacturer/Device ID(5)(6)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID(5)(6)	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Disable QPI	**FFh**					
Set Burst with Wrap	**77h**	dummy	dummy	dummy	W6-W4, xxxxx	(D7-D0)
Enable Reset	**66h**					
Reset	**99h**					
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0	(D7-D0) (2)	
Global Block Lock	**7Eh**	A23-A16	A15-A8	A7-A0		
Global Block Unlock	**98h**	A23-A16	A15-A8	A7-A0		

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The Status Register contents/Device ID/ASP contnets will repeat continuously until CS# terminates the instruction.
3. Write Status Register-1(01h) can also be used to program Status Register-1&2, see secion 10.2.4.
4. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
5. See Table 8 Manufacturer and Device Identification table for device ID information.
6. This feature is available upon special order. Please contact Shanghai Fudan Microelectronics Group Co., Ltd for details.
7. Security Sector Address:
   Security Sector 0: A23-A16 = 00h; A15-A8 = 00h; A7-A0 = byte address
   Security Sector 1: A23-A16 = 00h; A15-A8 = 01h; A7-A0 = byte address
   Security Sector 2: A23-A16 = 00h; A15-A8 = 10h; A7-A0 = byte address
   Security Sector 3: A23-A16 = 00h; A15-A8 = 11h; A7-A0 = byte address
8. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
9. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)
10. Quad SPI address input format:
    DQ_0 = A20, A16, A12, A8, A4, A0, M4, M0
    DQ_1 = A21, A17, A13, A9, A5, A1, M5, M1
    DQ_2 = A22, A18, A14, A10, A6, A2, M6, M2
    DQ_3 = A23, A19, A15, A11, A7, A3, M7, M3

    Set Burst with Wrap input format:
    DQ_0 = x, x, x, x, x, x, W4, x
    DQ_1 = x, x, x, x, x, x, W5, x
    DQ_2 = x, x, x, x, x, x, W6, x
    DQ_3 = x, x, x, x, x, x, x, x
11. Quad SPI data input/output format:
    DQ_0 = (D4, D0, …)
    DQ_1 = (D5, D1, …..)
    DQ_2 = (D6, D2, …..)
    DQ_3 = (D7, D3, …..)
12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)
13. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)
14. QPI Command Address, Data input/output format:

CLK#	0	1	2	3	4	5	6	7	8	9	10	11
DQ_0	C4	C0	A20	A16	A12	A8	A4	A0	D4	D0	D4	D0
DQ_1	C5	C1	A21	A17	A13	A9	A5	A1	D5	D1	D5	D1
DQ_2	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2
DQ_3	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3

15. The number of dummy clocks is controlled by Latency code bits LC[1:0] in SR2.

10.2. Instruction Description

10.2.1. Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 13) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Sectors instruction. The Write Enable **(**WREN**)** instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

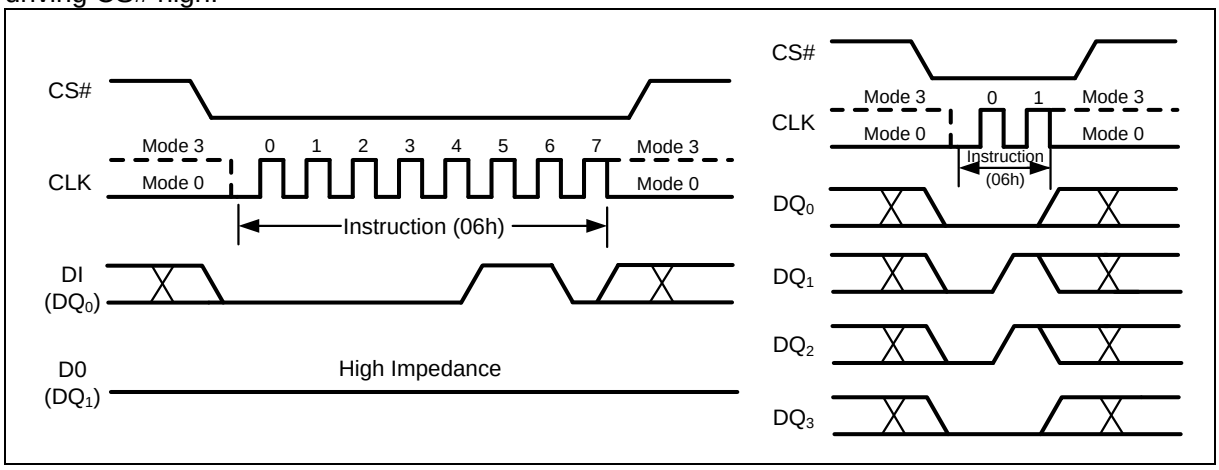


Figure 13 Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

10.2.2. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 9.1, 9.2, 9.3 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 14) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

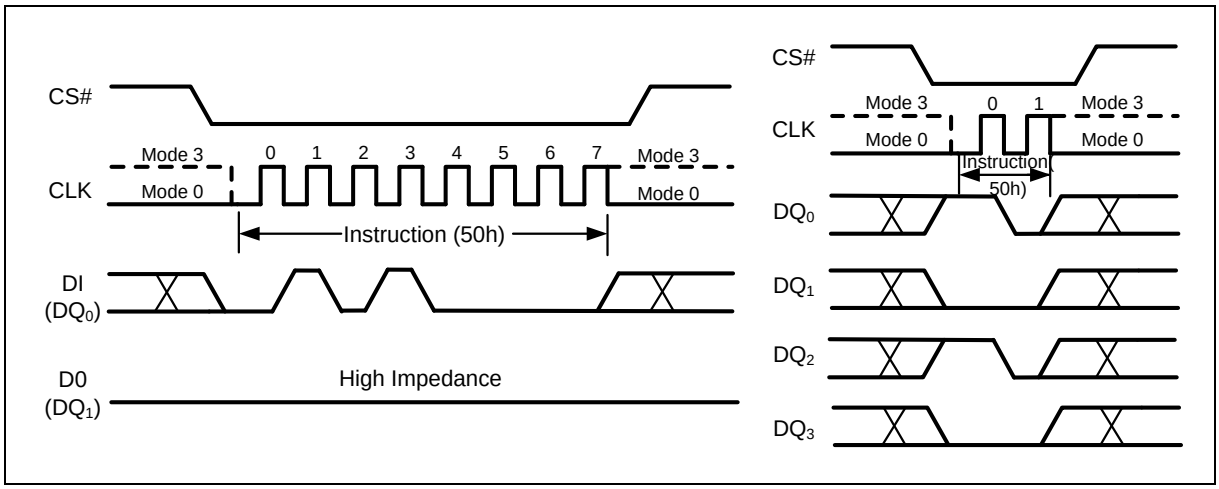


Figure 14 Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

10.2.3. Write Disable (WRDI) (04h)

The Write Disable (WRDI) instruction (Figure 15) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Sectors, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

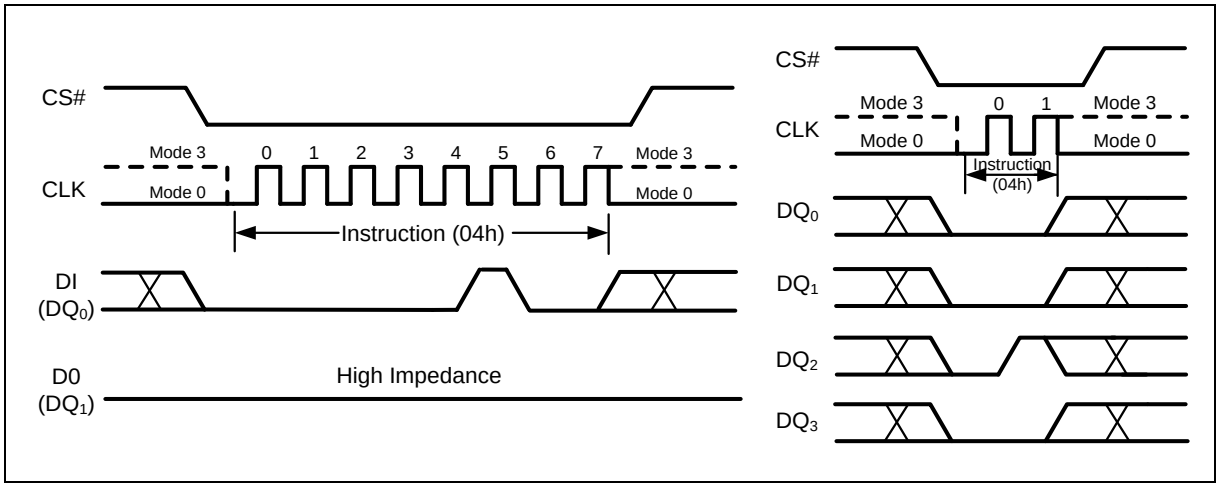


Figure 15 Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

10.2.4. Read Status Register-1 (RDSR1) (05h), Status Register-2 (RDSR2) (35h) & Status Register-3 (RDSR3) (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 16. Refer to section 9.1, 9.2, 9.3 for Status Register description.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 17. The instruction is completed by driving CS# high.

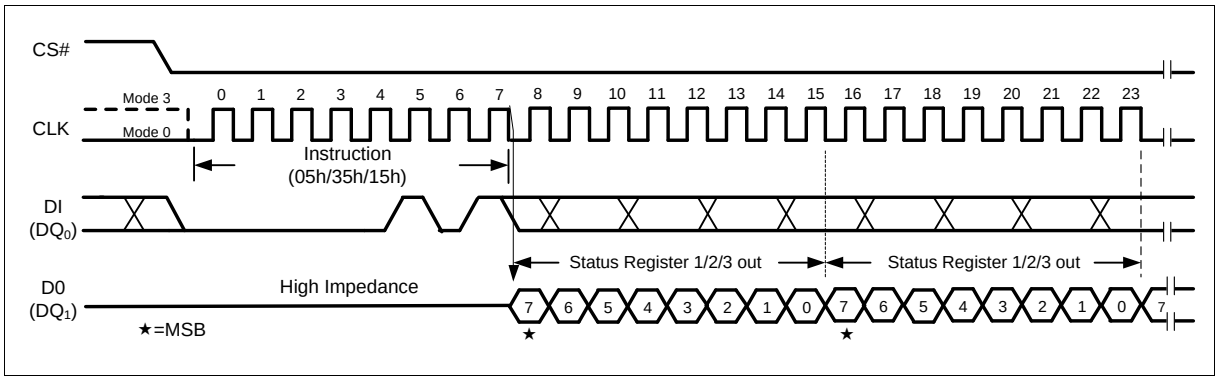


Figure 16 Read Status Register Instruction (SPI Mode)

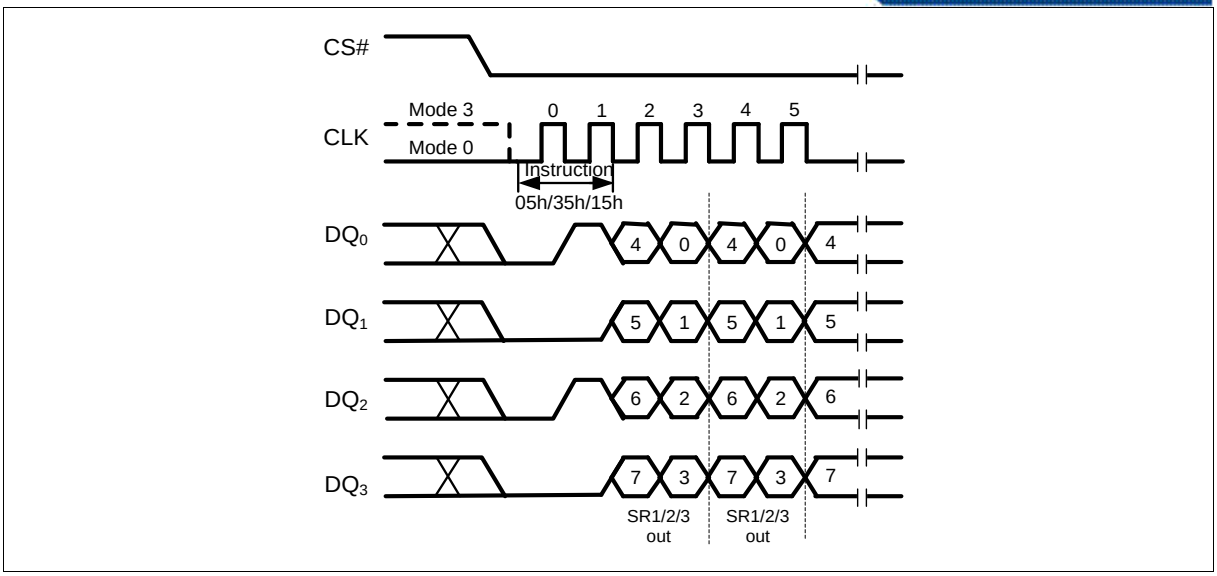


Figure 17 Read Status Register Instruction (QPI Mode)

10.2.5. Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Register to be written. The writable Status Register bits include: SRP, TB, CMP, BP[2:0] in Status Register-1; LC[1:0], LB[1:0], QE, in Status Register-2; HOLD/RST, DRV1, DRV0 & WPS in Status Register-3. All other Status Register bit locations are read-only and will not be affected by Write Status Register instruction.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 18 and Figure 19.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). Upon power off or the execution of Software Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “11.6 AC Electrical Characteristics”). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See “11.6 AC Electrical Characteristics”). WIP bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to 0 when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Refer to section 9.1, 9.2, 9.3 for Status Register description. Factory default for all status Register bits are 0.

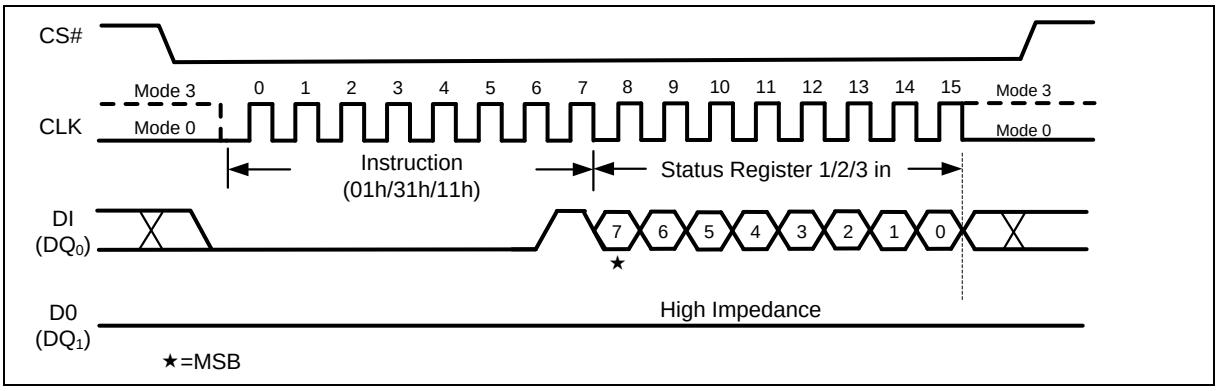


Figure 18 Write Status Register-1/2/3 Instruction (SPI Mode)

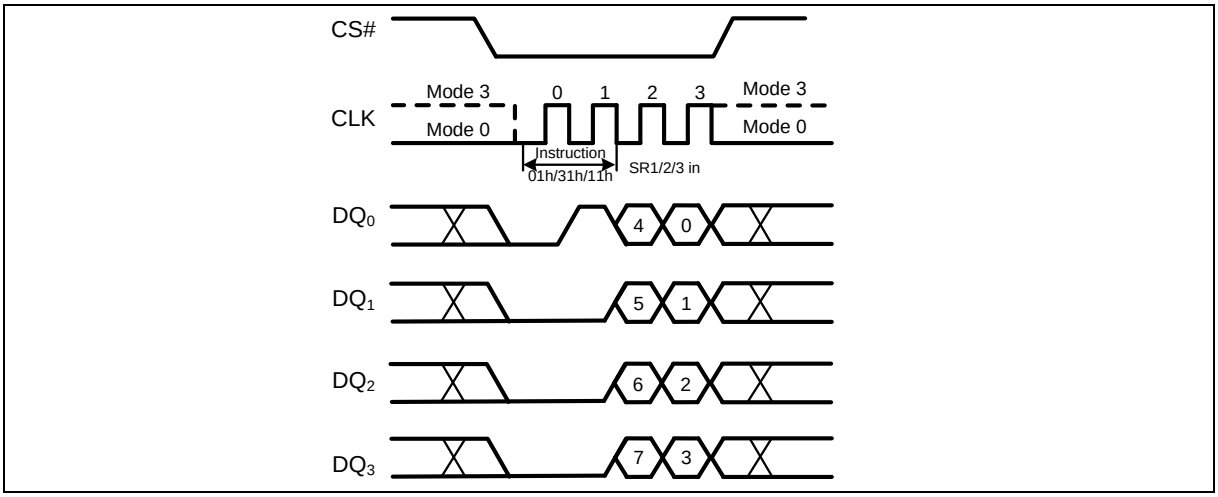


Figure 19 Write Status Register-1/2/3 Instruction (QPI Mode)

10.2.6. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 20. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see “11.6 AC Electrical Characteristics”).

The Read Data (03h) instruction is only supported in Standard SPI mode.

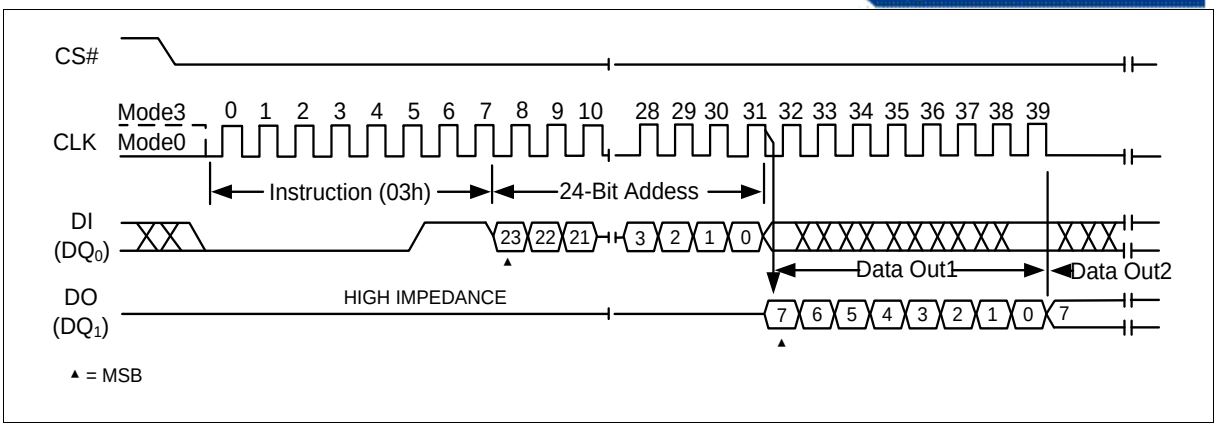


Figure 20 Read Data Instruction (SPI Mode only)

10.2.7. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see "11.6 AC Electrical Characteristics"). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 21. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a "don't care".

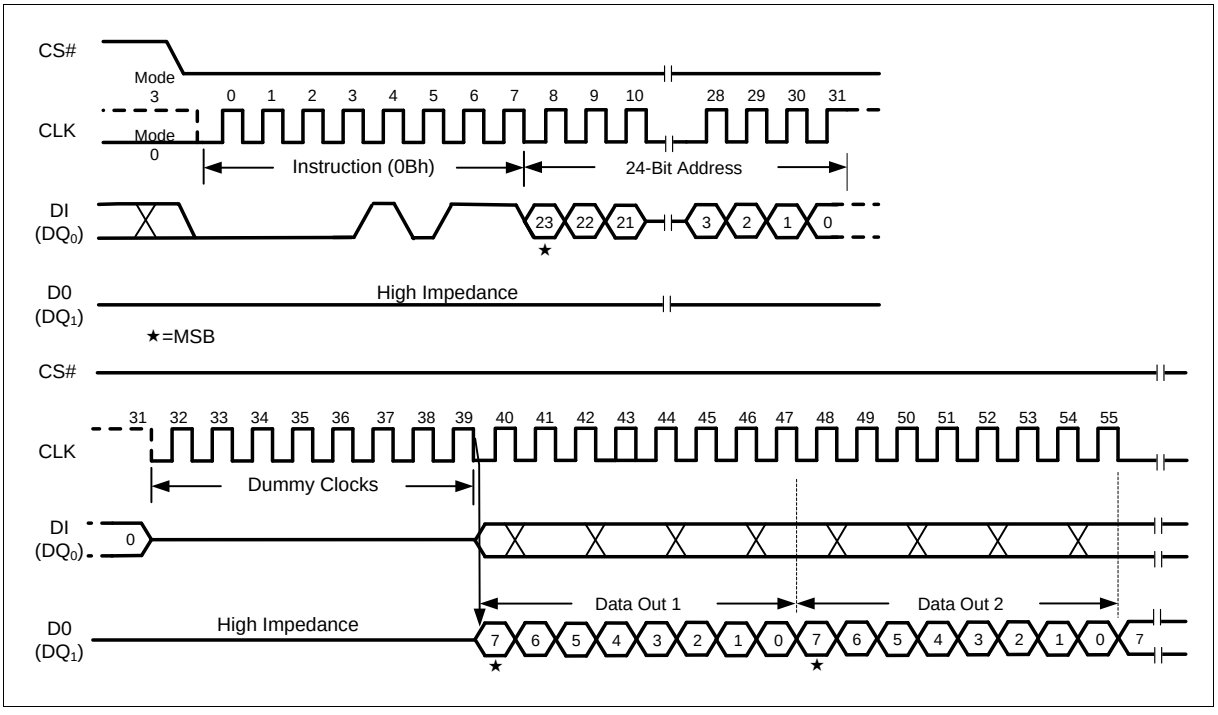


Figure 21 Fast Read Instruction (SPI Mode)

Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is controlled by Latency code bits LC[1:0] in SR2 to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Latency code bits LC[1:0] setting, the number of dummy clocks can be configured as either 4, 6, 8 or 10. The default number of dummy clocks upon power up or after a Reset instruction is 6.

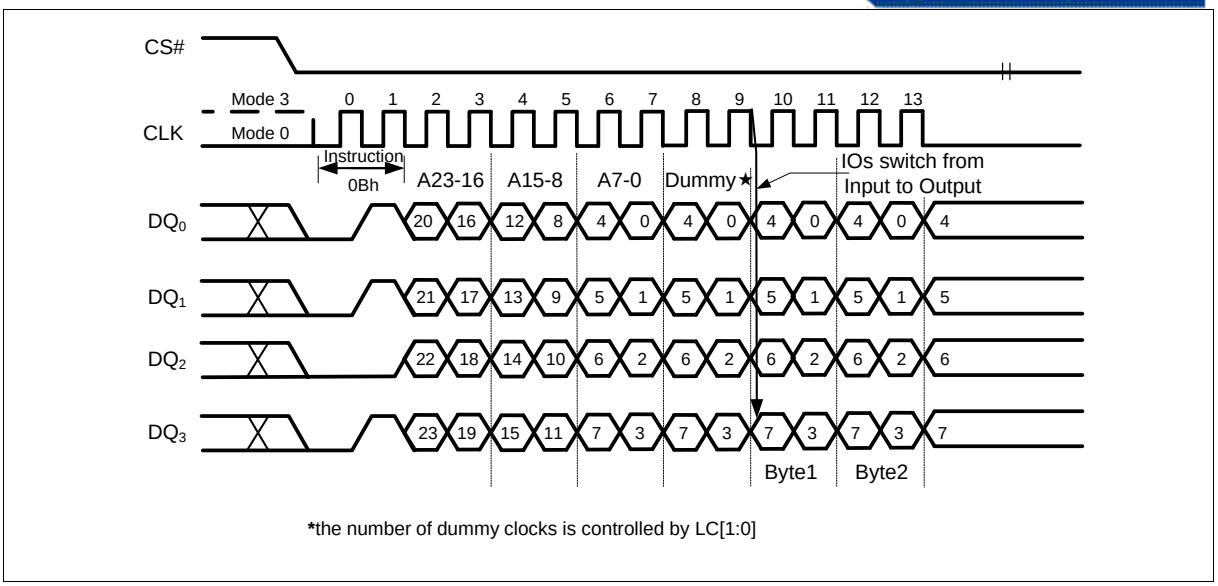


Figure 22 Fast Read Instruction (QPI Mode)

10.2.8. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the FM25Q128 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see “11.6 AC Electrical Characteristics”). For Fast Read Dual Output instruction, there are zero or eight dummy cycles required after the last address bit is shifted into DI before data begins shifting out of DQ_0 and DQ_1. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

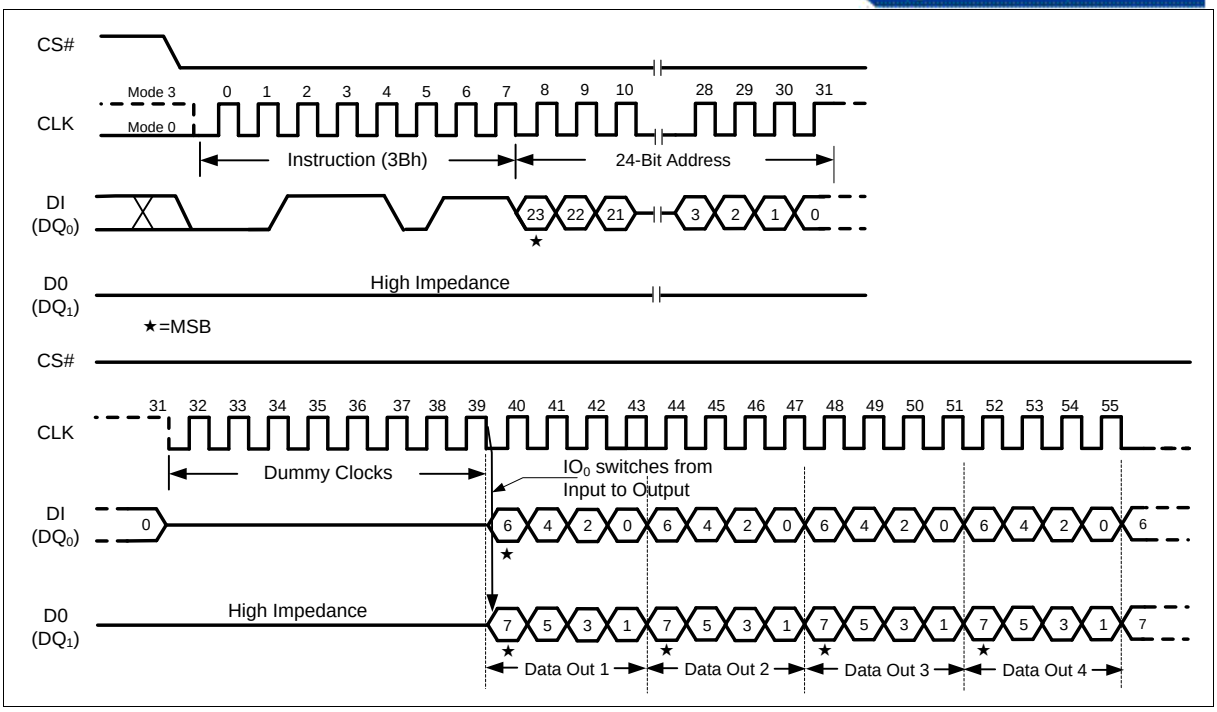


Figure 23 Fast Read Dual Output Instruction (SPI Mode only)

10.2.9. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, DQ_0, DQ_1, DQ_2, and DQ_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE must equal 1). The Fast Read Quad Output Instruction allows data to be transferred from the FM25Q128 at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see “11.6 AC Electrical Characteristics”). For Fast Read Quad Output instruction, there are zero or eight dummy cycles required after the last address bit is shifted into DI before data begins shifting out of DQ_0, DQ_1, DQ_2 and DQ_3. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

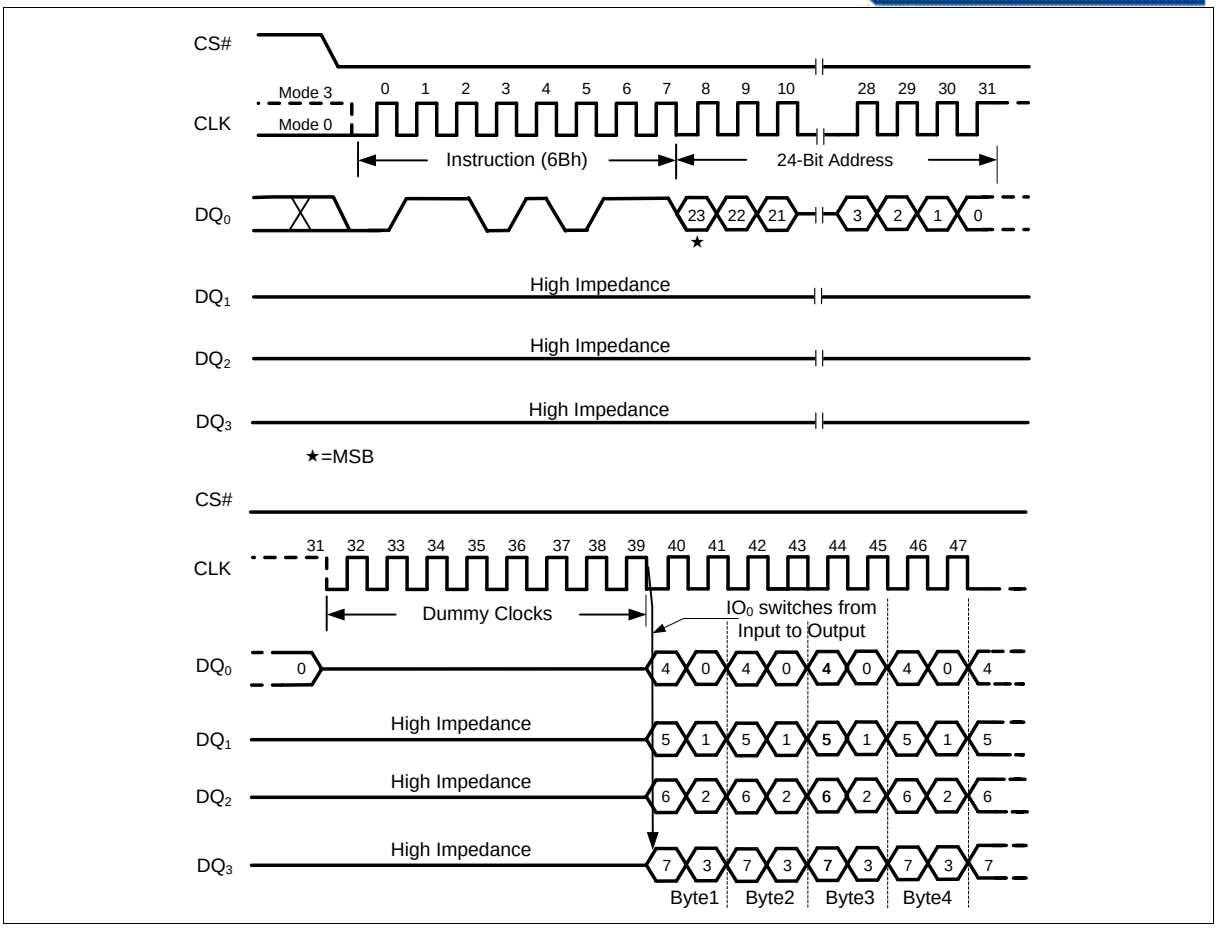


Figure 24 Fast Read Quad Output Instruction (SPI Mode only)

10.2.10. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits A23-A0 two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Fast Read Dual I/O instruction can operate at the highest possible frequency of F_R (see "11.6 AC Electrical Characteristics"). This is accomplished by adding "dummy cycles" after the last address bits are shifted in DQ_0 and DQ_1. The number of dummy cycles is controlled by LC[1:0]. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 25. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 26. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do

not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next

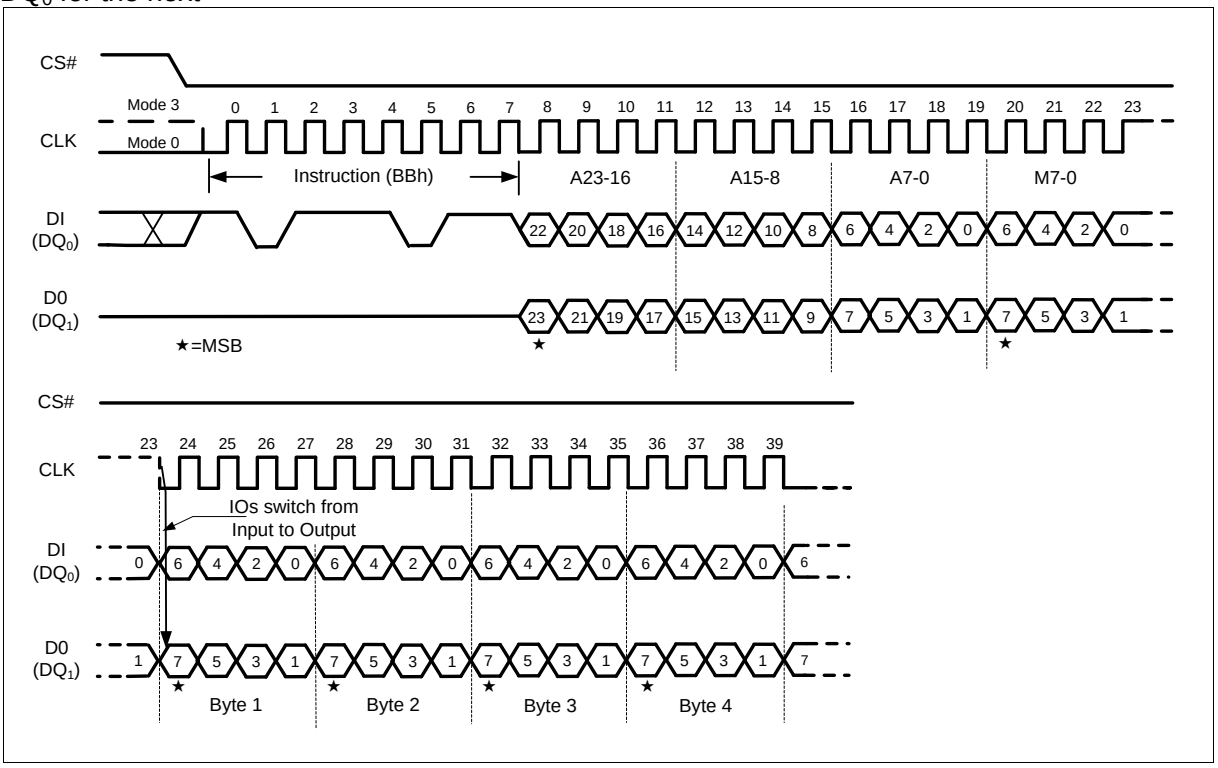


Figure 25 Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

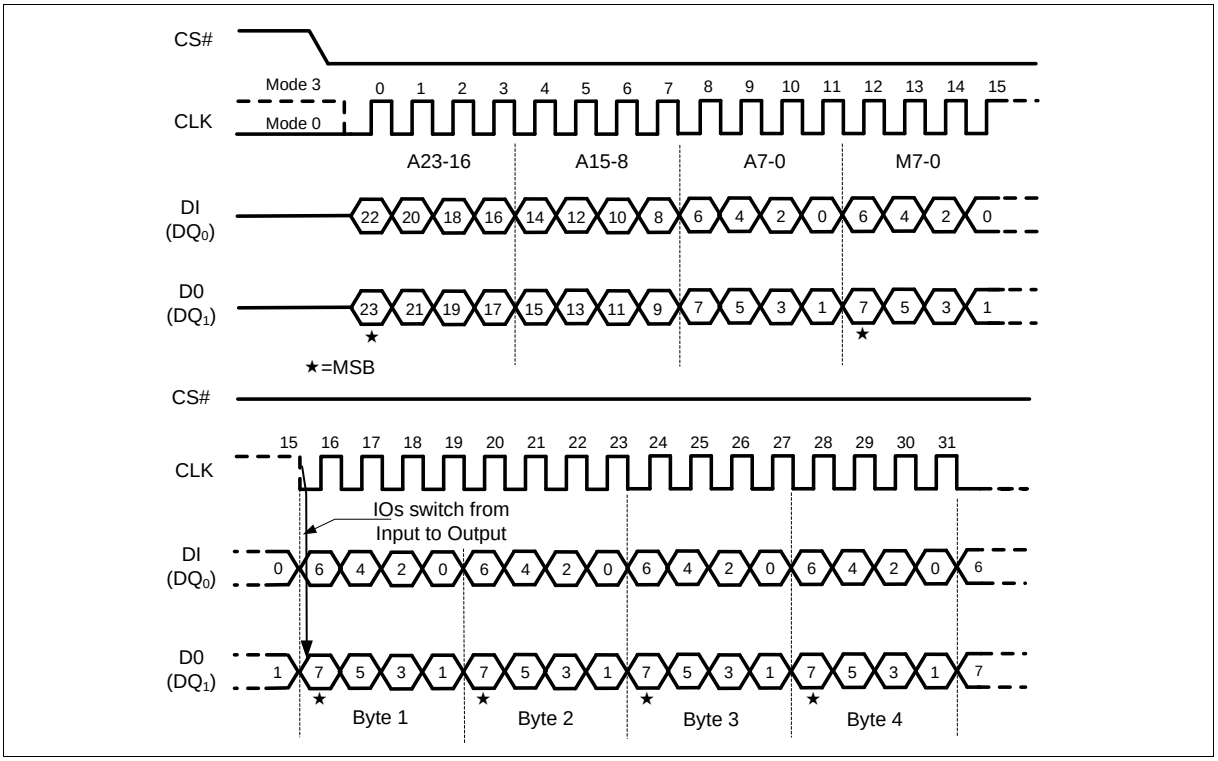


Figure 26 Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

10.2.11. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins DQ_0, DQ_1, DQ_2 and DQ_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

The Fast Read Quad I/O instruction can operate at the highest possible frequency of F_R (see "11.6 AC Electrical Characteristics"). This is accomplished by adding "dummy cycles" after the last address bits are shifted in DQ_0, DQ_1, DQ_2 and DQ_3. The number of dummy cycles is controlled by LC[1:0]. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 27. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 28. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

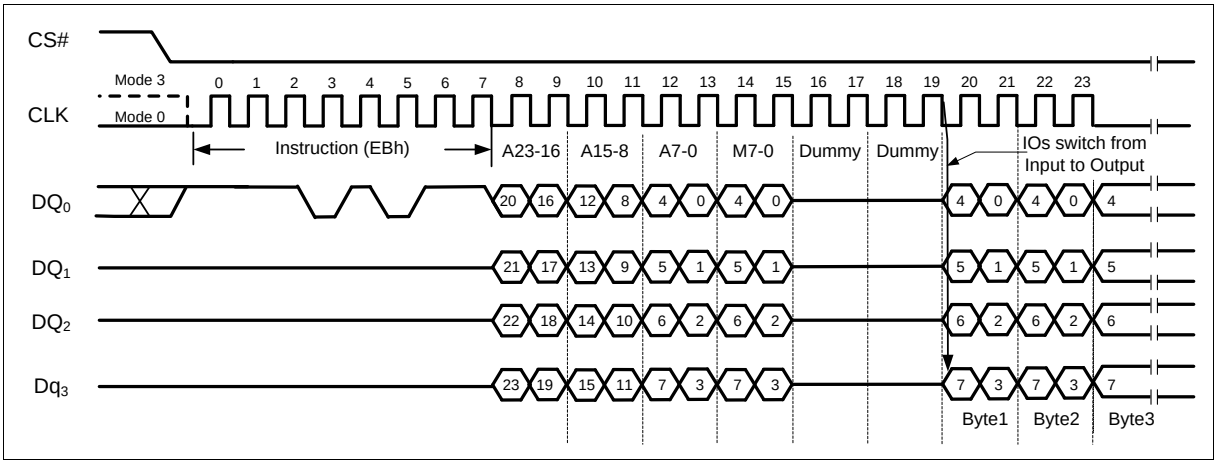


Figure 27 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

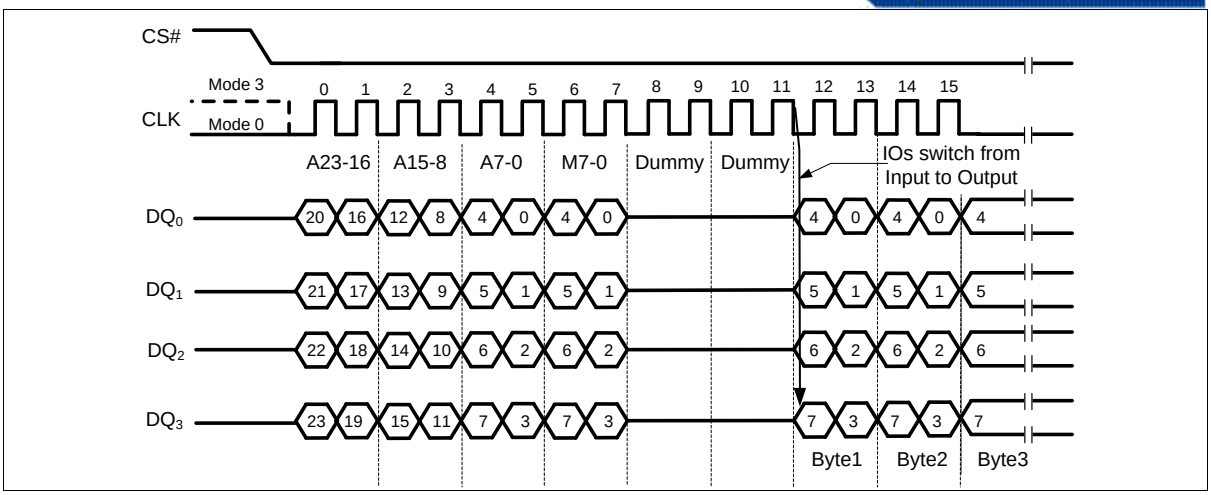


Figure 28 Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "10.2.14 Set Burst with Wrap (77h)" for detail descriptions.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 29. When QPI mode is enabled, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages for details.

"Wrap Around" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages for details.

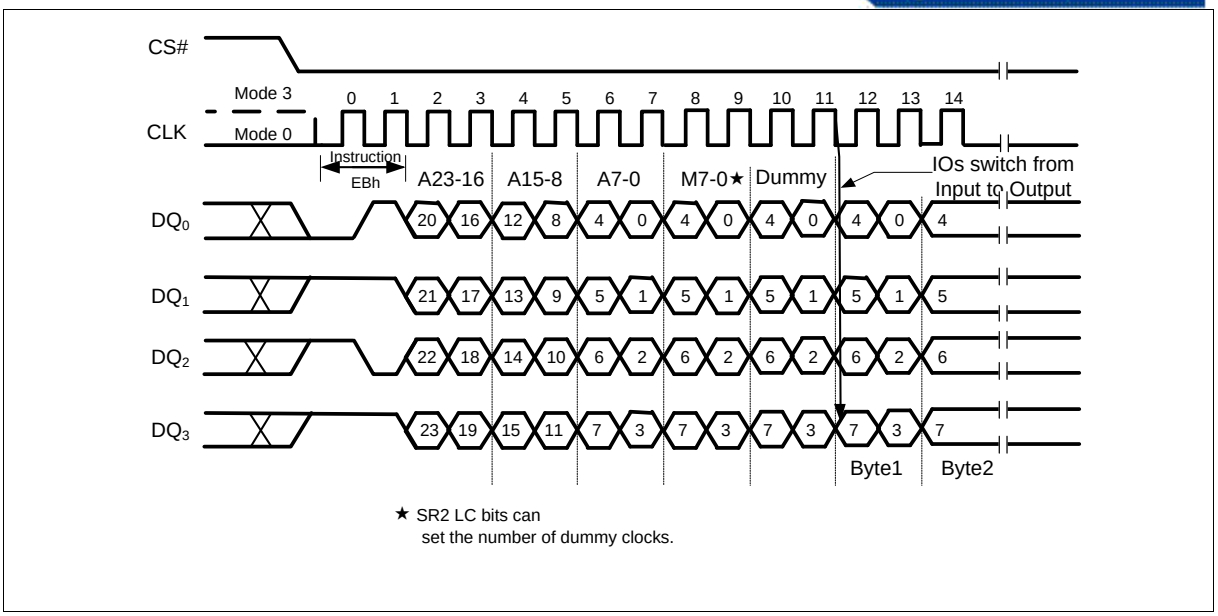


Figure 29 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)

10.2.12. Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0. The number of dummy cycles for Word Read Quad I/O (E7h) instruction refers to table. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 30. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the E7h instruction code, as shown in Figure 31. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

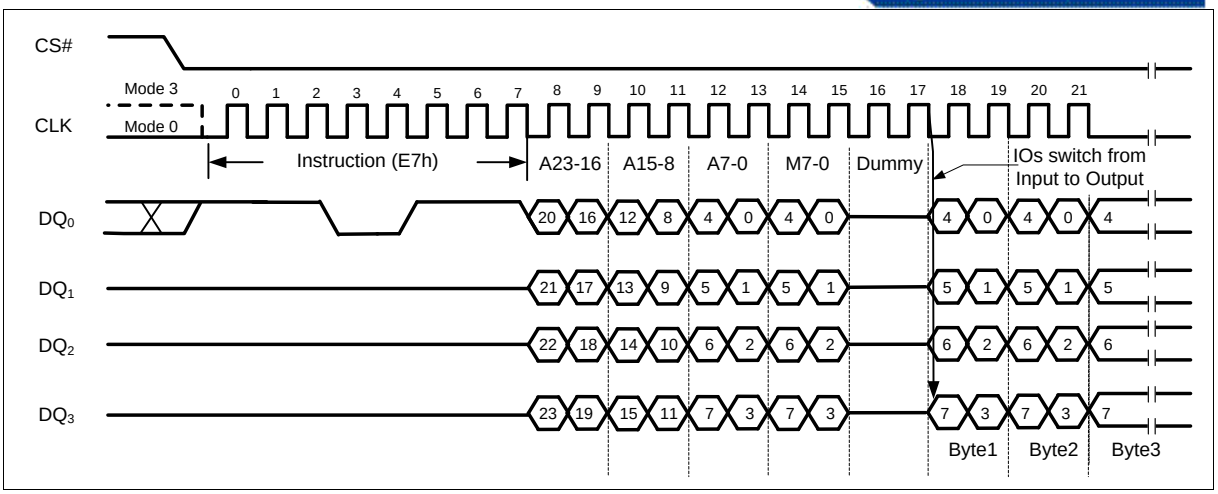


Figure 30 Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

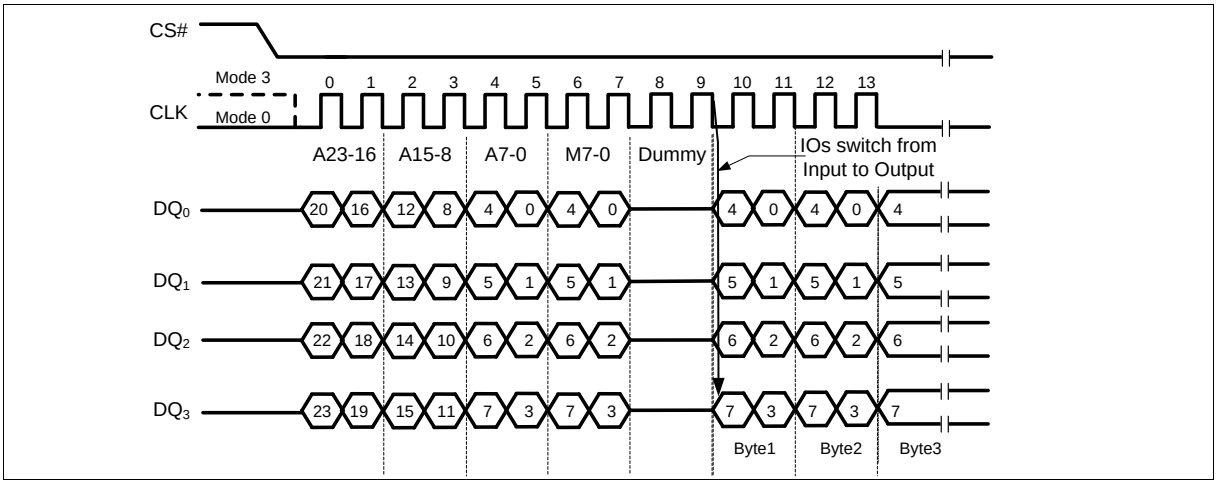


Figure 31 Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See 10.2.14 Set Burst with Wrap (77h)" for detail descriptions.

10.2.13. Octal Word Read Quad I/O (E3h)

The Octal Word Read Quad I/O (E3h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lower four Address bits (A0, A1, A2, A3) must equal 0. The number of dummy cycles for Octal Word Read Quad I/O (E3h) instruction refers to table . The Quad I/O dramatically reduces the instruction overhead allowing even faster random access for code execution (XIP). The Quad Enable bit (QE) of Status Register-2 must be set to enable the Octal Word Read Quad I/O Instruction.

Octal Word Read Quad I/O with "Continuous Read Mode"

The Octal Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits M7-M0 after the input Address bits A23-A0, as shown in Figure 32. The upper nibble of the (M7-4) controls the length of the next Octal Word Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the E3h instruction code, as shown in Figure 33. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

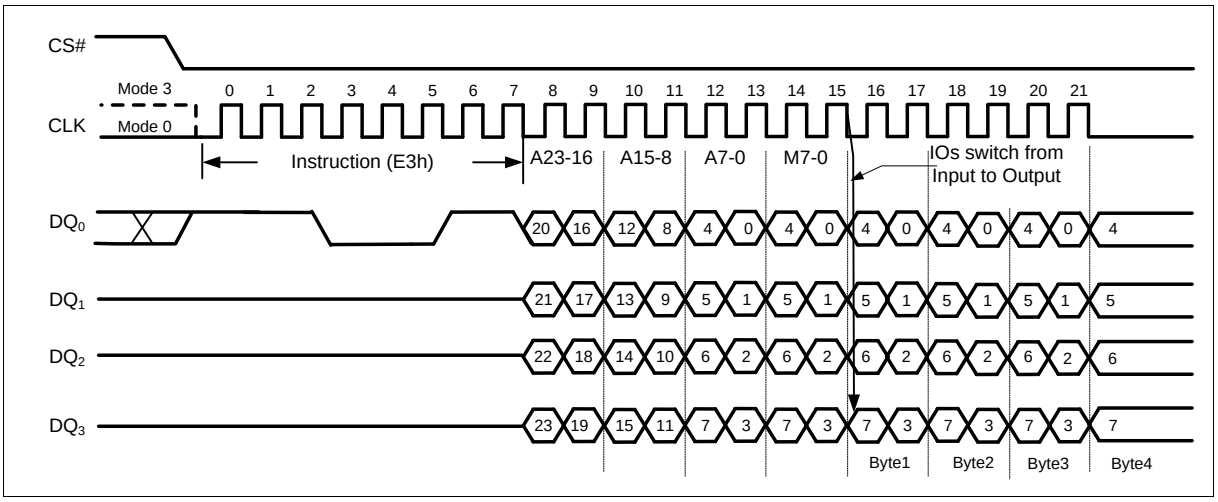


Figure 32 Octal Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

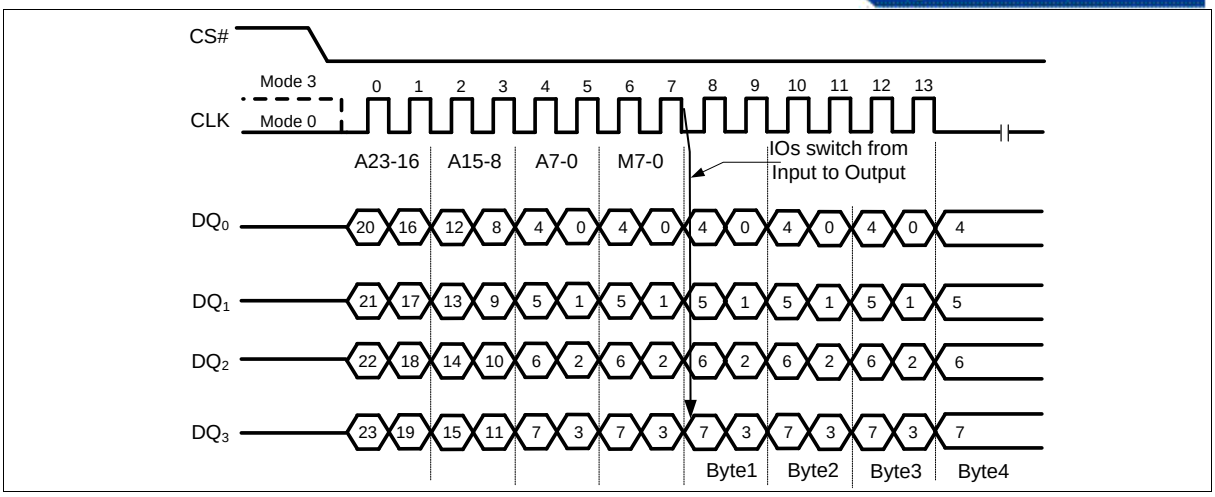


Figure 33 Octal Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

10.2.14. Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” , “Word Read Quad I/O” and “Burst Read with Wrap” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the CS# pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 34. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O” and “Word Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions.

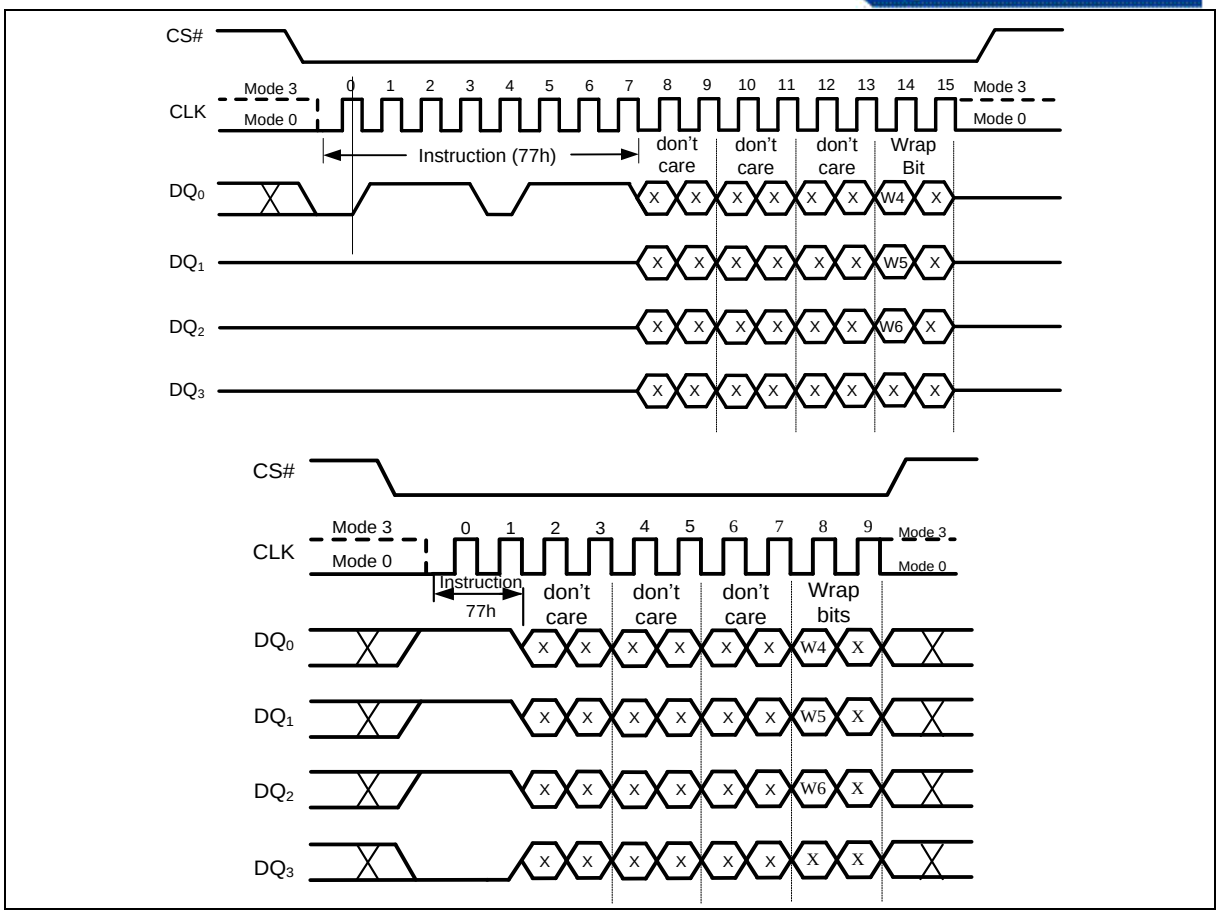


Figure 34 Set Burst with Wrap Instruction for SPI Mode(Up) or QPI Mode(Down)

10.2.15. Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "02h" followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 35 and Figure 36.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{PP} (See "11.6 AC Electrical Characteristics"). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page

Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP2, BP1, and BP0) bits.

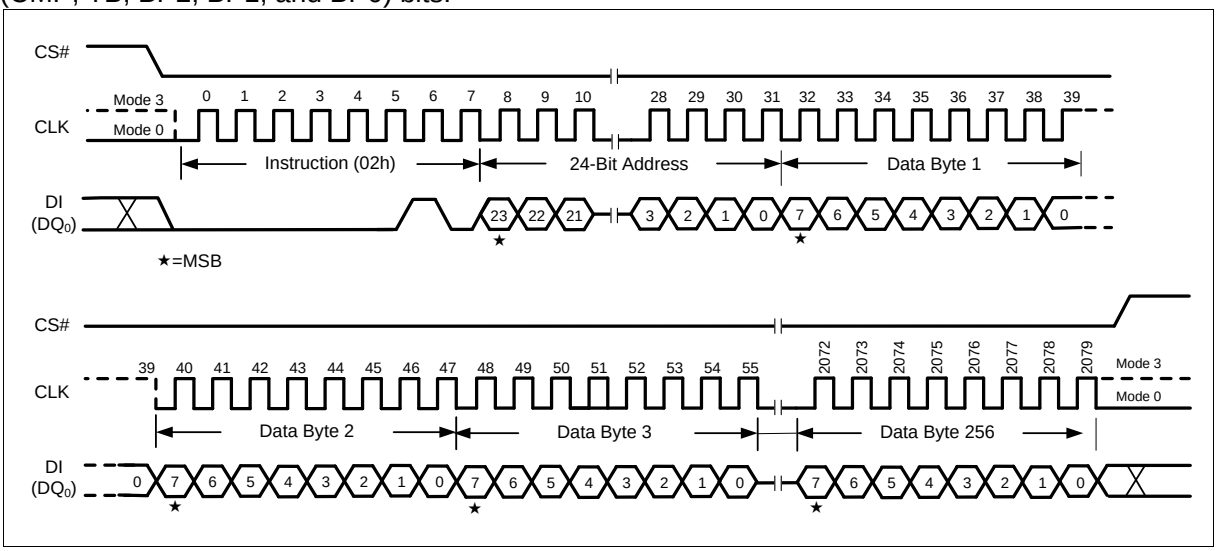


Figure 35 Page Program Instruction (SPI Mode)

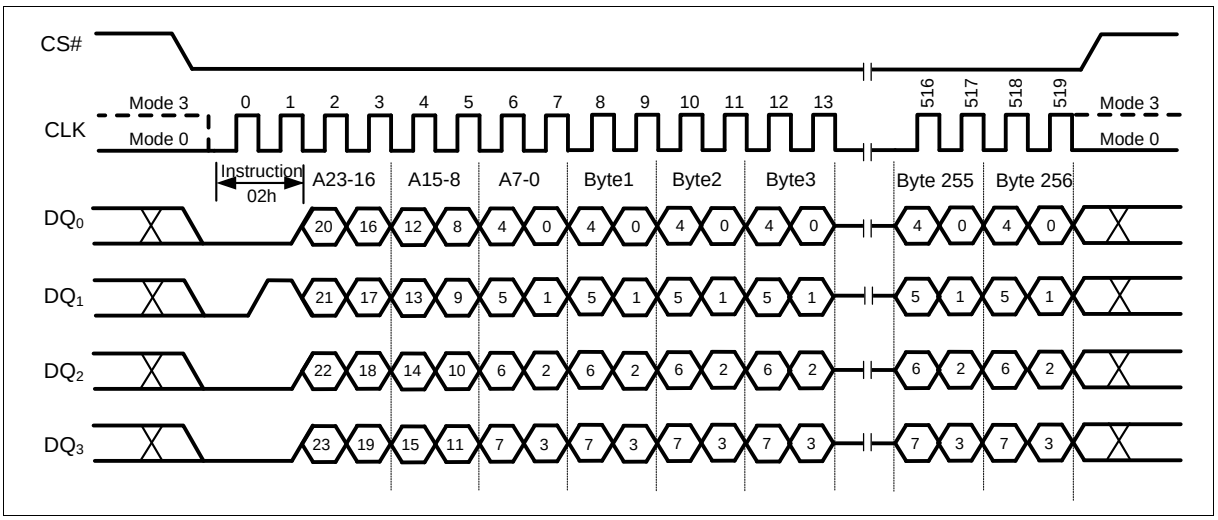


Figure 36 Page Program Instruction (QPI Mode)

10.2.16. Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2, and DQ_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “32h” followed by a 24-bit address A23-A0 and at least one data byte, into the DQ pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 37.

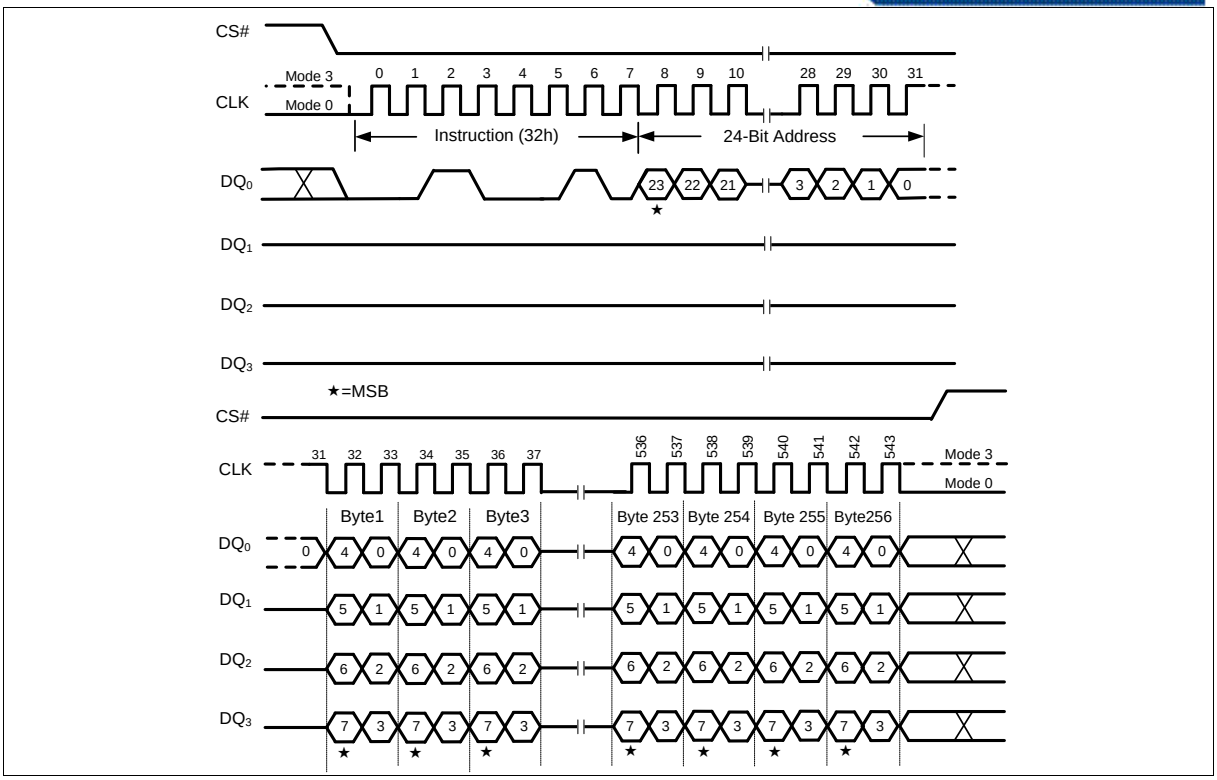


Figure 37 Quad Input Page Program Instruction (SPI Mode only)

10.2.17. Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address A23-A0. The Sector Erase instruction sequence is shown in Figure 38 & Figure 39.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See “11.6 AC Electrical Characteristics”). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP2, BP1, and BP0) bits (see Table 6 Status Register Memory Protection table).

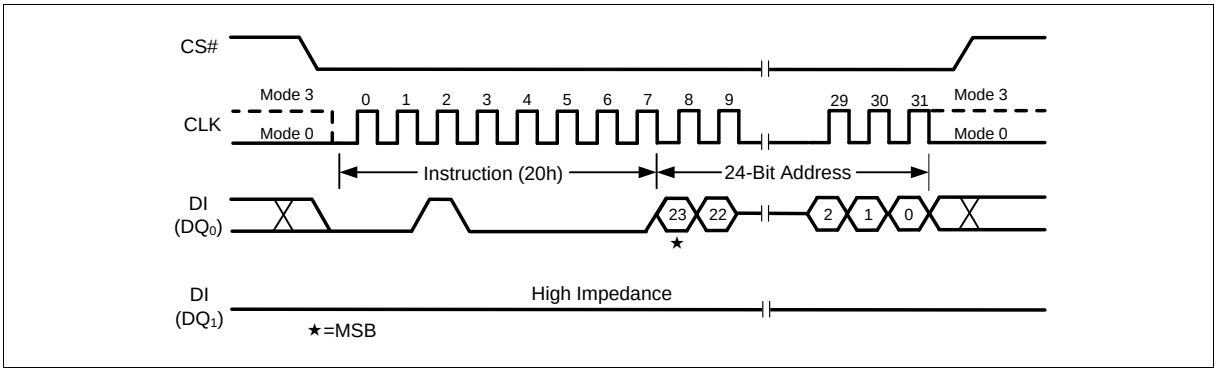


Figure 38 Sector Erase Instruction (SPI Mode)

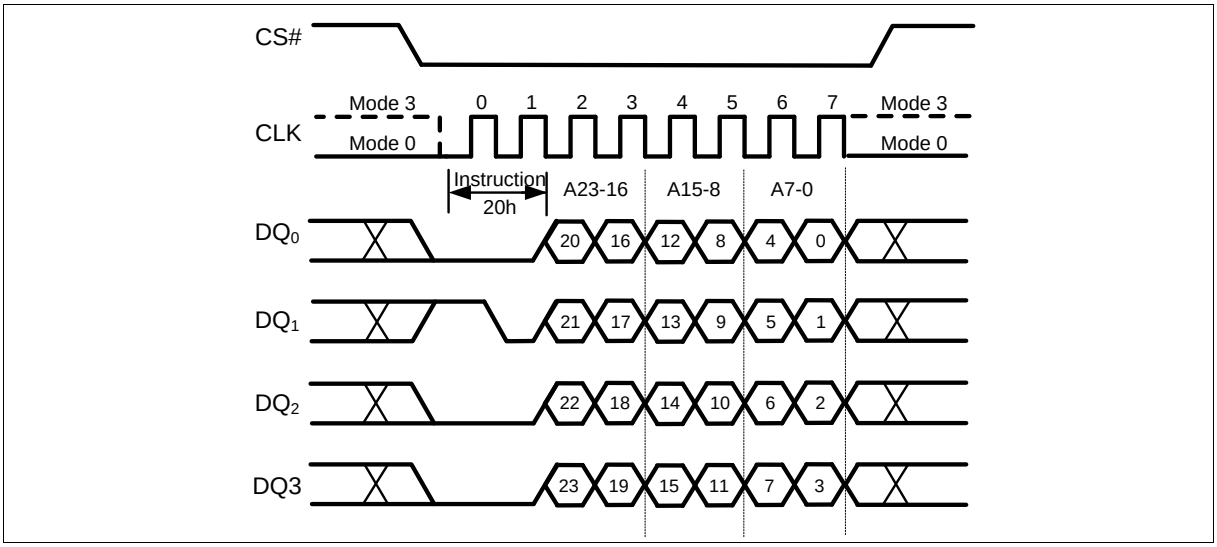


Figure 39 Sector Erase Instruction (QPI Mode)

10.2.18. 32KB Block Erase (BE32) (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “52h” followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 40 & Figure 41.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See “11.6 AC Electrical Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP2, BP1, and BP0) bits (see Table 6 Status Register Memory Protection table).

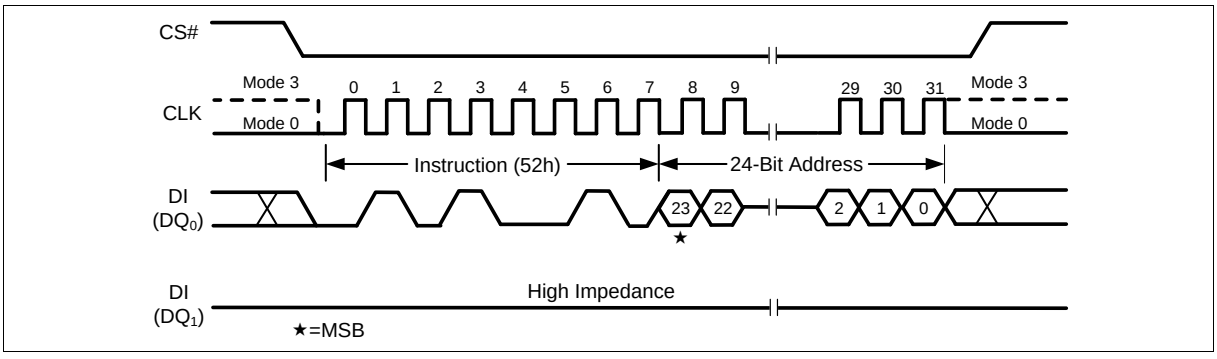


Figure 40 32KB Block Erase Instruction (SPI Mode)

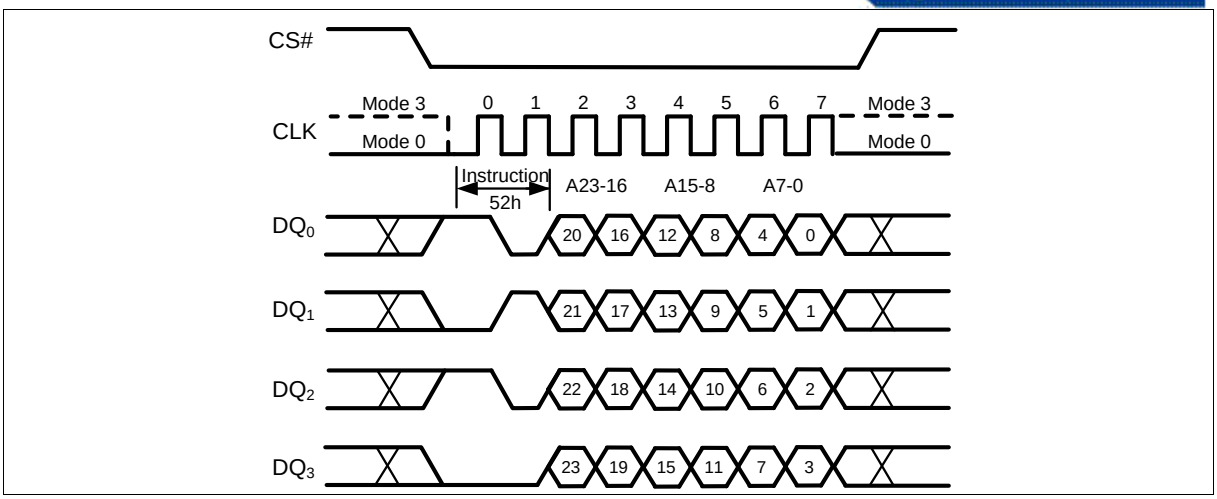


Figure 41 32KB Block Erase Instruction (QPI Mode)

10.2.19. 64KB Block Erase (BE) (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 42 & Figure 43.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See 11.6 AC Electrical Characteristics"). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP2, BP1, and BP0) bits (see Table 6 Status Register Memory Protection table).

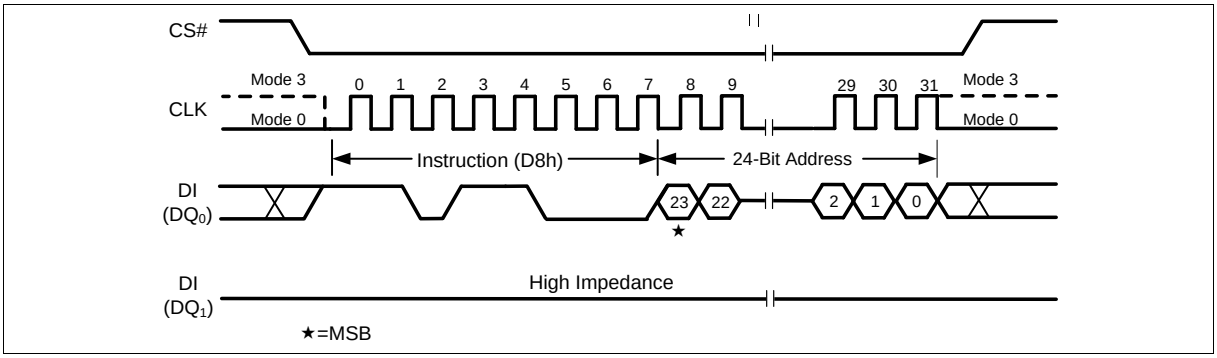


Figure 42 64KB Block Erase Instruction (SPI Mode)

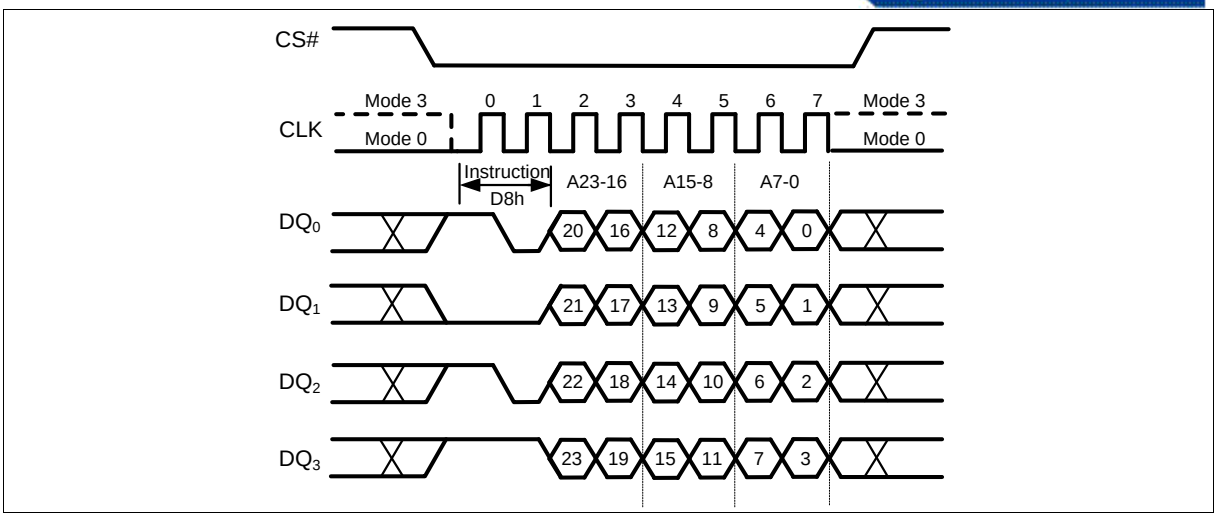


Figure 43 64KB Block Erase Instruction (QPI Mode)

10.2.20. Chip Erase (CE) (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 44.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See “11.6 AC Electrical Characteristics”). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, TB, BP2, BP1, and BP0) bits.

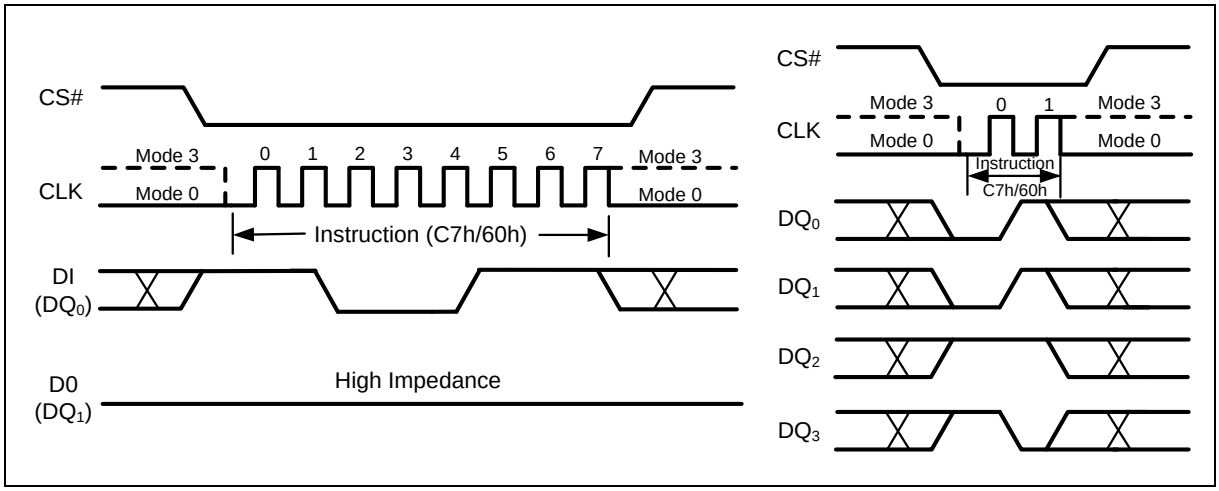


Figure 44 Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

10.2.21. Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See I_{CC1} and I_{CC2} in "11.4 DC Electrical Characteristics"). The instruction is initiated by driving the CS# pin low and shifting the instruction code "B9h" as shown in Figure 45 & Figure 46.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See "11.6 AC Electrical Characteristics"). While in the power-down state only the Release from Power- down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

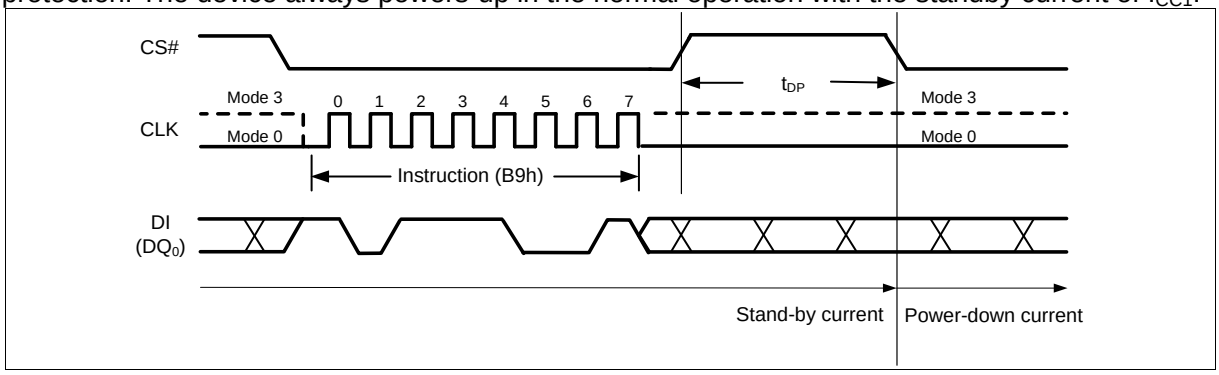


Figure 45 Deep Power-down Instruction (SPI Mode)

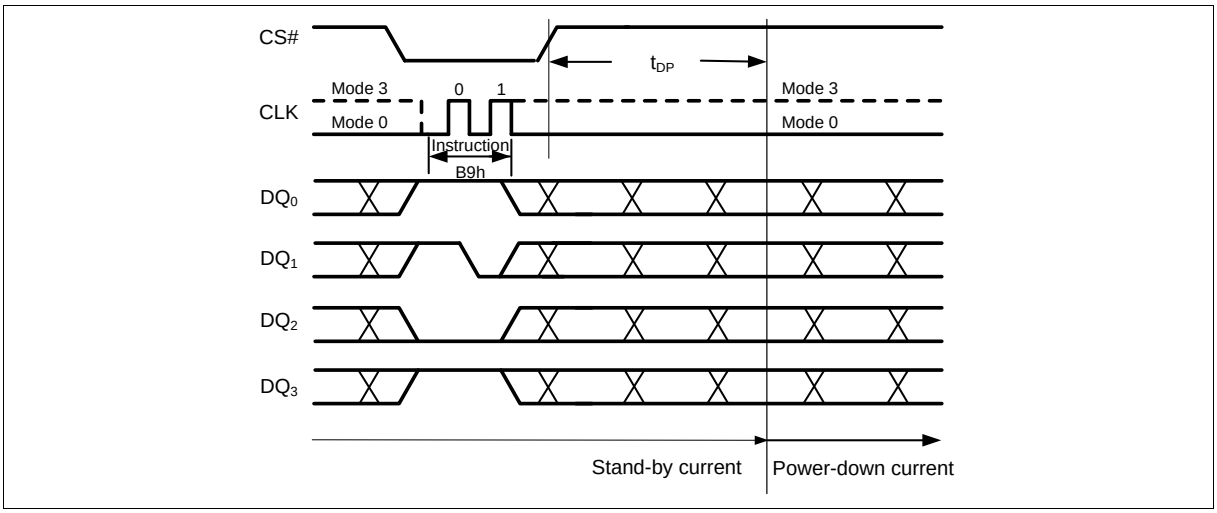


Figure 46 Deep Power-down Instruction (QPI Mode)

10.2.22. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 47 & Figure 48. Release from power-down will take the time duration of t_{RES1} (See "11.6 AC Electrical

Characteristics") before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 47 & Figure 48. The Device ID value for the FM25Q128 is listed in Table 8 Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 49 & Figure 50, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See "11.6 AC Electrical Characteristics"). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effect on the current cycle.

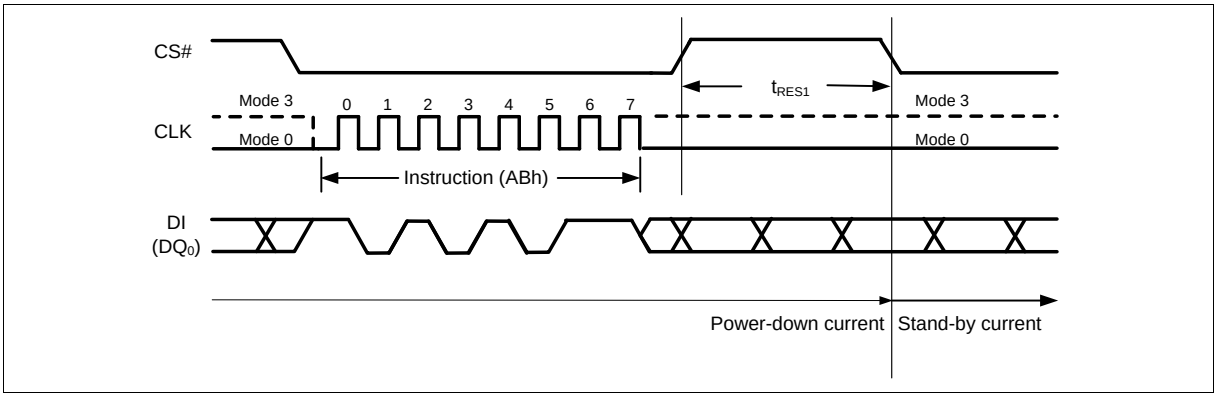


Figure 47 Release Power-down Instruction (SPI Mode)

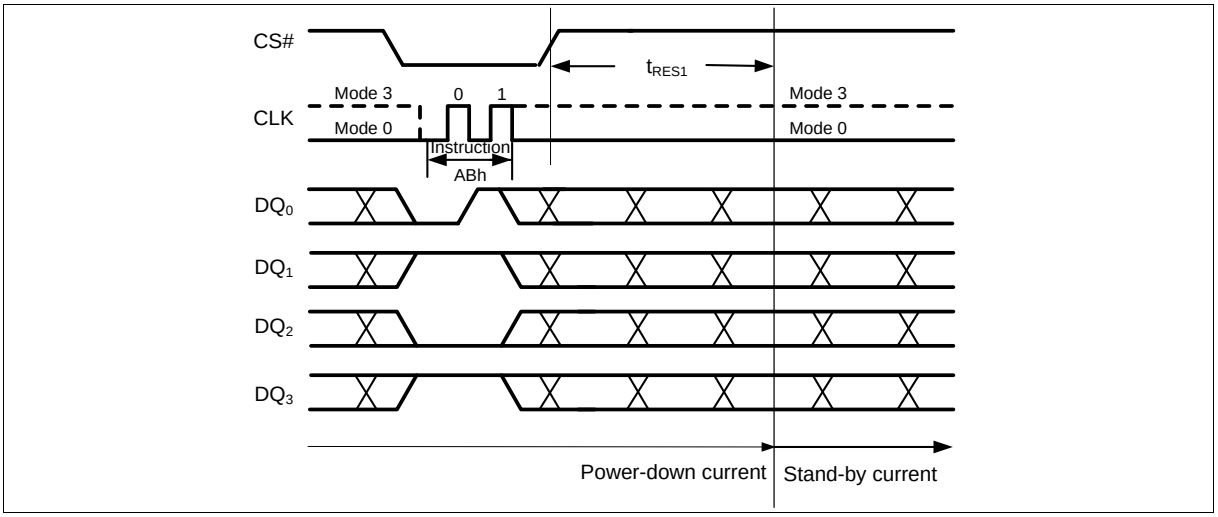


Figure 48 Release Power-down Instruction (QPI Mode)

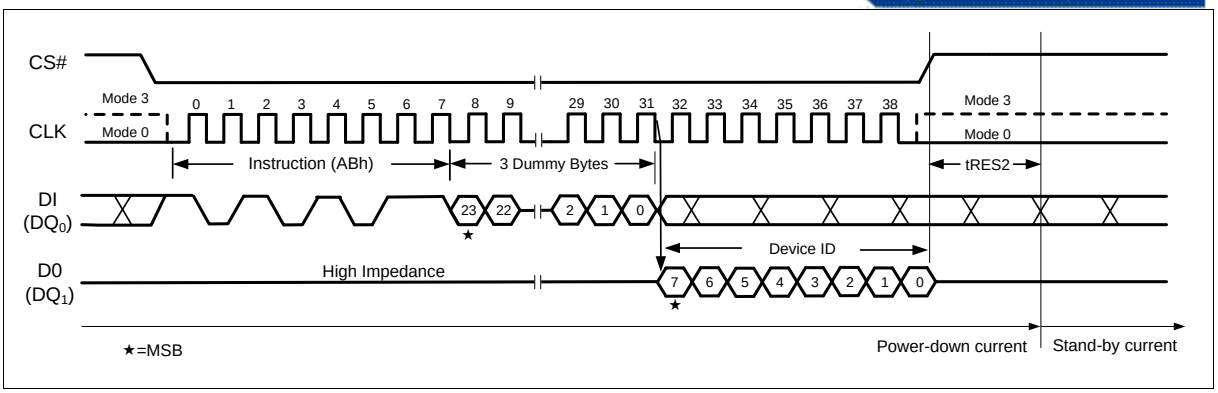


Figure 49 Release Power-down / Device ID Instruction (SPI Mode)

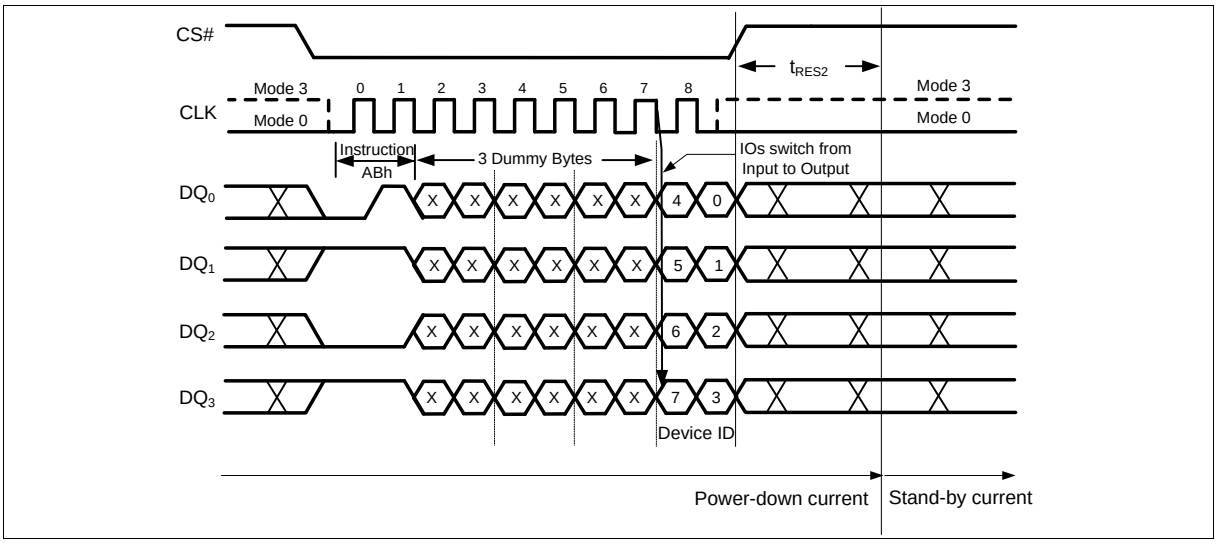


Figure 50 Release Power-down / Device ID Instruction (QPI Mode)

10.2.23. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 51 & Figure 52. The Device ID value for the FM25Q128 is listed in Table 8 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

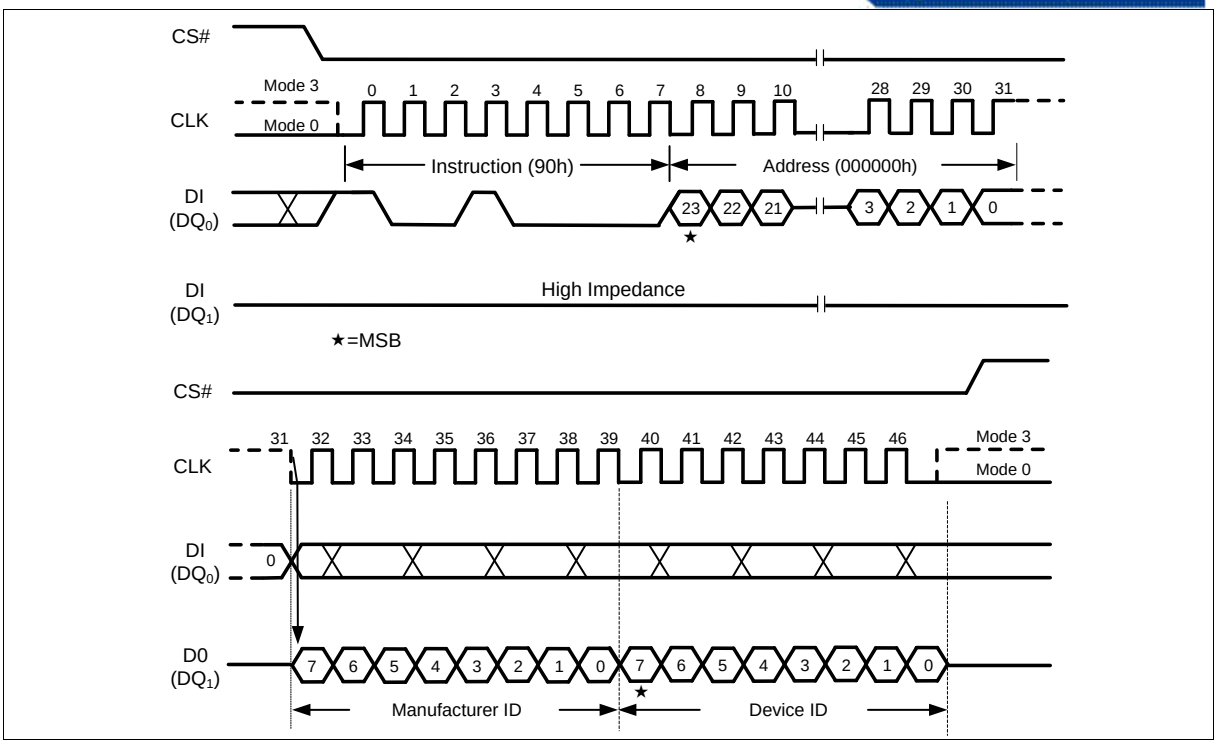


Figure 51 Read Manufacturer / Device ID Instruction (SPI Mode)

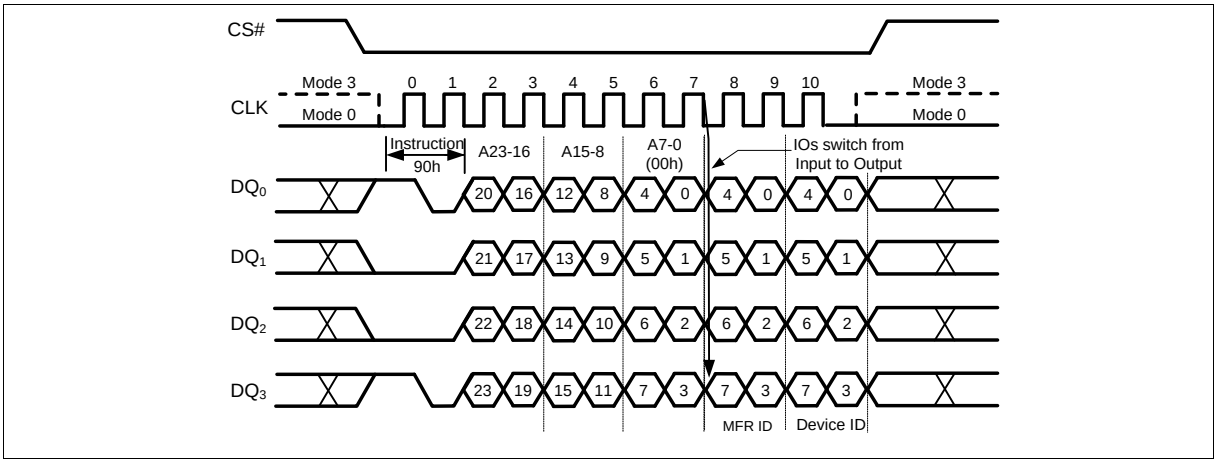


Figure 52 Read Manufacturer / Device ID Instruction (QPI Mode)

10.2.24. Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “92h” followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 53. The Device ID value for the FM25Q128 is listed in Table 8 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously,

alternating from one to the other. The instruction is completed by driving CS# high.

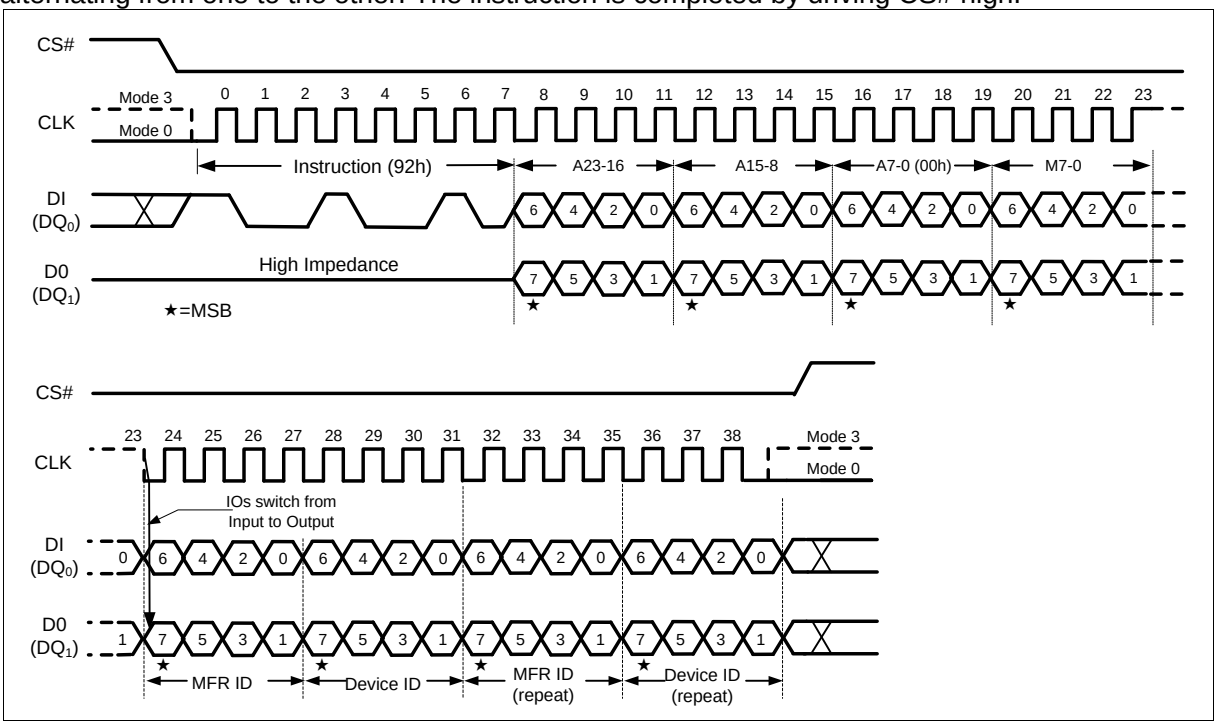


Figure 53 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

Note:
The "Continuous Read Mode" bits M7-M0 must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

10.2.25. Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "94h" followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits and then four clock dummy cycles, with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 54. The Device ID value for the FM25Q128 is listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

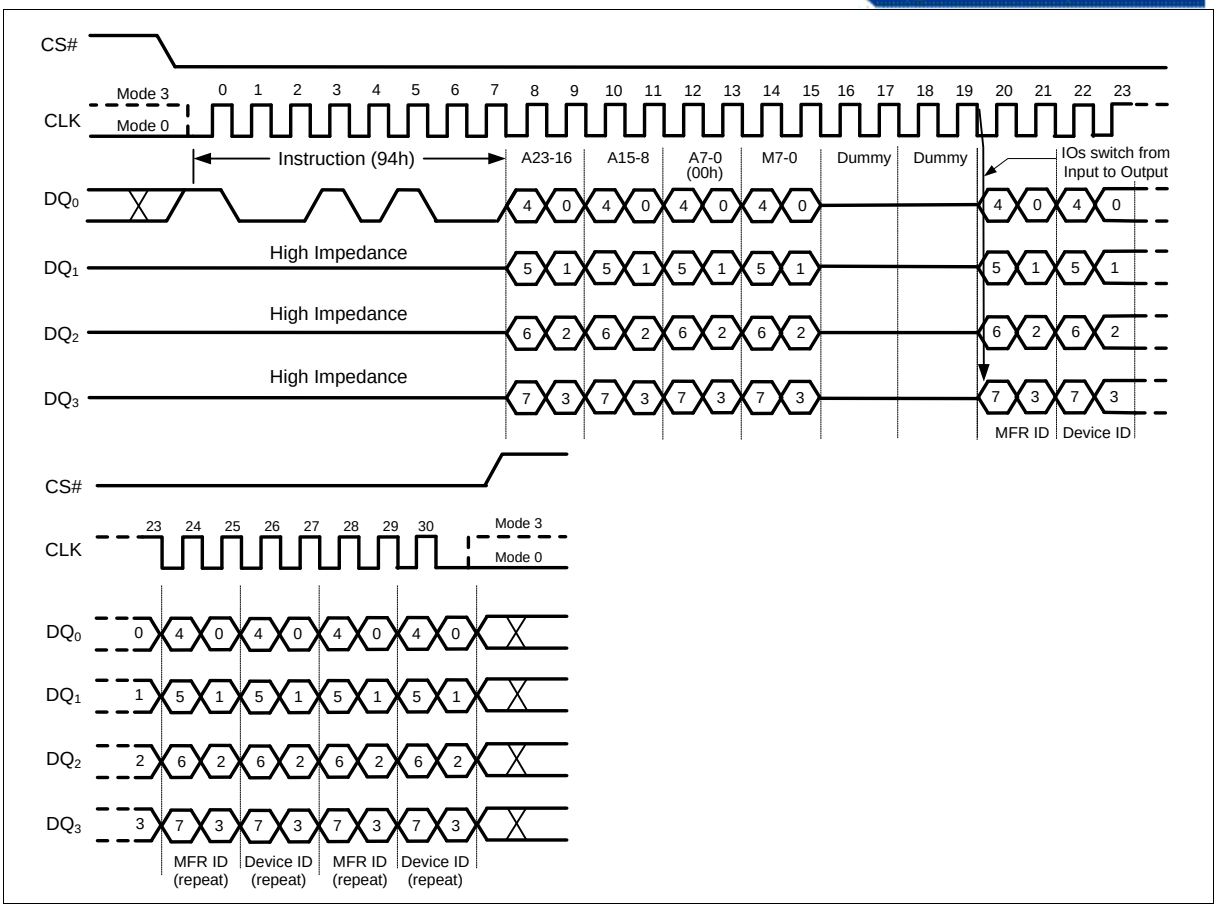


Figure 54 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

Note:
The “Continuous Read Mode” bits M7-M0 must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

10.2.26. Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each FM25Q128 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in Figure 55.

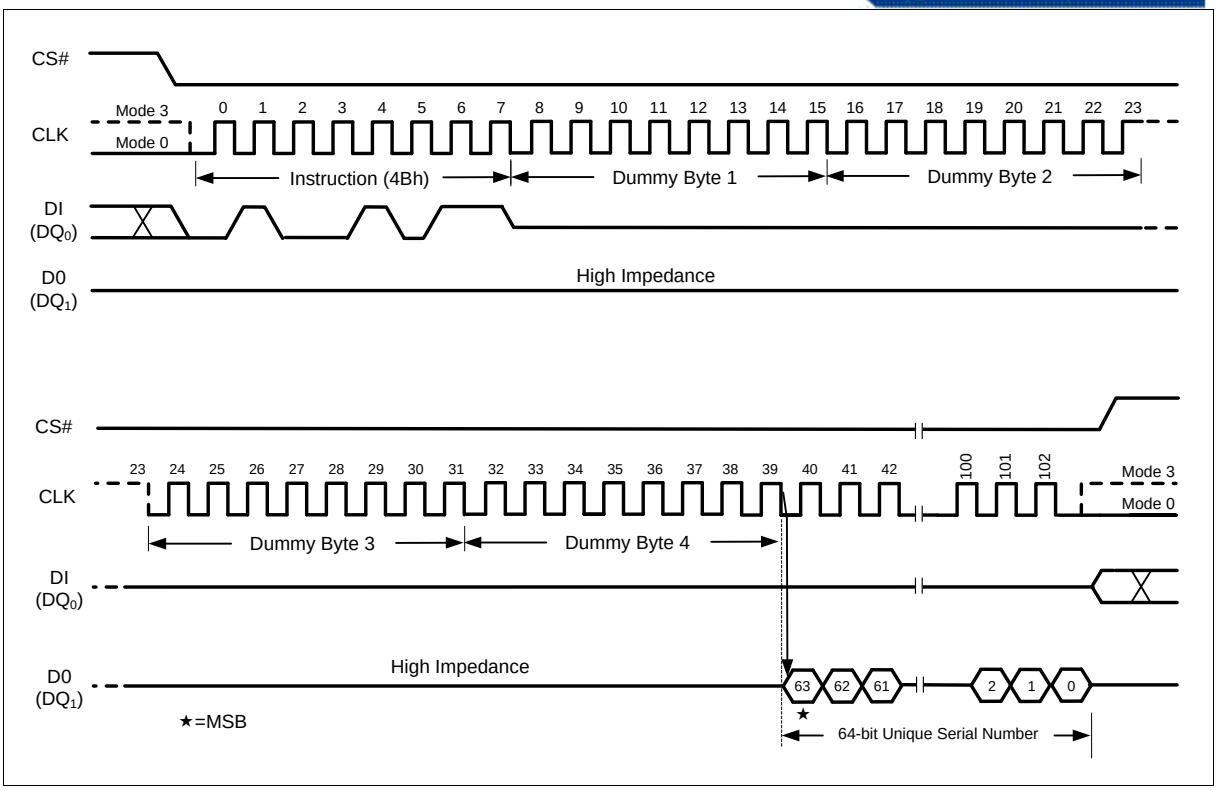


Figure 55 Read Unique ID Number Instruction (SPI Mode only)

10.2.27. Read JEDEC ID (9Fh)

For compatibility reasons, the FM25Q128 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 56 & Figure 57. For memory type and capacity values refer to Table 8 Manufacturer and Device Identification table.

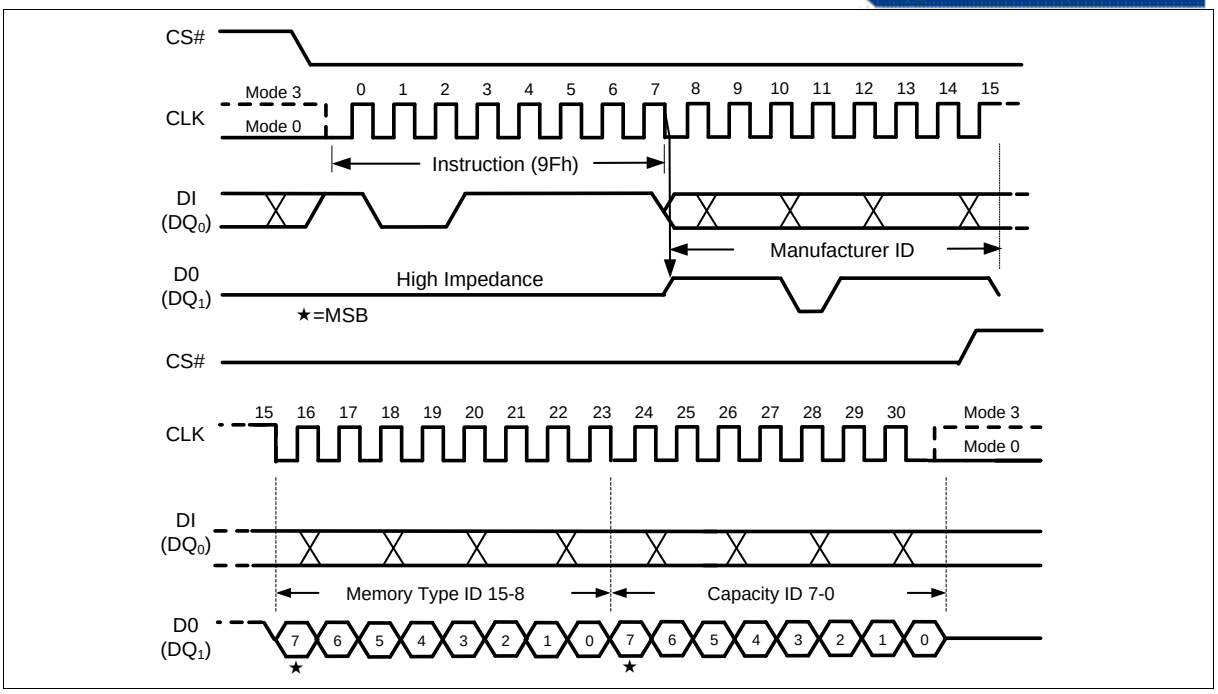


Figure 56 Read JEDEC ID Instruction (SPI Mode)

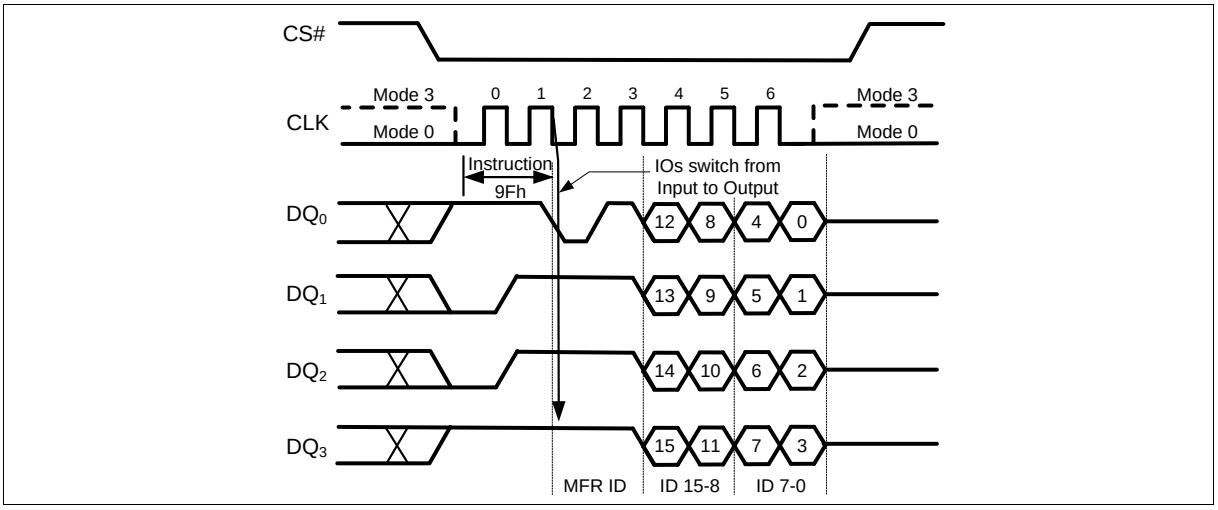


Figure 57 Read JEDEC ID Instruction (QPI Mode)

10.2.28. Read SFDP Register (5Ah)

The FM25Q128 features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard 1.0 that is published in 2011.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 58. For SFDP register values and descriptions, refer to the following SFDP Definition table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

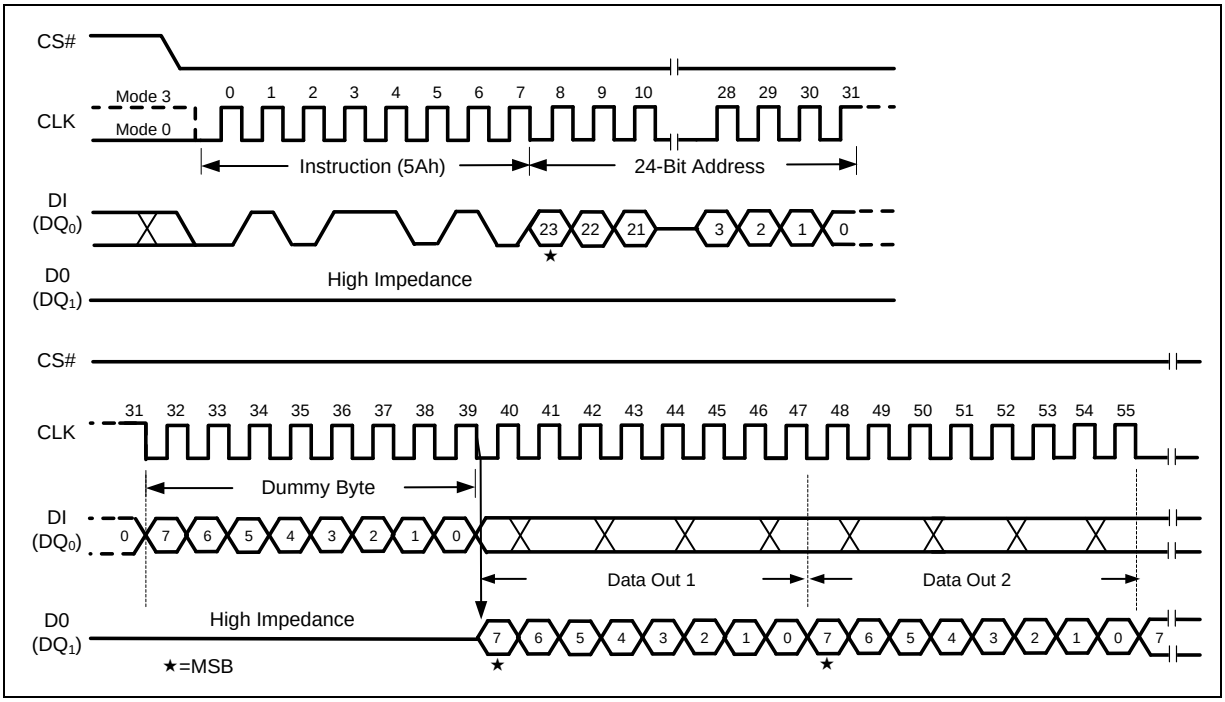


Figure 58 Read SFDP Register Instruction

Serial Flash Discoverable Parameter (JEDEC Revision 1.0) Definition Table

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
00h	53h	SFDP Signature	SFDP Signature = 50444653h
01h	46h	SFDP Signature	
02h	44h	SFDP Signature	
03h	50h	SFDP Signature	
04h	00h	SFDP Minor Revision Number	JEDEC Revision 1.0
05h	01h	SFDP Major Revision Number	
06h	00h	Number of Parameter Headers (NPH)	1 Parameter Header
07h	FFh	Reserved	
08h	00h	PID(3)(0): ID Number	00h = JEDEC specified
09h	00h	PID(0): Parameter Table Minor Revision Number	JEDEC Revision 1.0
0Ah	01h	PID(0): Parameter Table Major Revision Number	
0Bh	09h	PID(0): Parameter Table Length	9 Dwords(2)
0Ch	80h	PID(0): Parameter Table Pointer (PTP) (A7-A0)	PID(0) Pointer = 000080h
0Dh	00h	PID(0): Parameter Table Pointer (PTP) (A15-A8)	
0Eh	00h	PID(0): Parameter Table Pointer (PTP) (A23-A16)	
0Fh	FFh	Reserved	
10h	FFh	Reserved	
...(1)	FFh	Reserved	
7Fh	FFh	Reserved	
80h	E5h	Bit[7:5]=111 Reserved Bit[4:3]=00 Non-volatile Status Register Bit[2]=1 Page Programmable Bit[1:0]=01 Supports 4KB Erase	
81h	20h	4K-Byte Erase Opcode	
82h	F1h	Bit[7] =1 Reserved	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
		Bit[6] =1 Supports (1-1-4) Fast Read Bit[5] =1 Supports (1-4-4) Fast Read Bit[4] =1 Supports (1-2-2) Fast Read Bit[3] =0 Not support Dual Transfer Rate Bit[2:1]=00 3-Byte/24-Bit Only Addressing Bit[0] =1 Supports (1-1-2) Fast Read	
83h	FFh	Reserved	
84h	FFh	Flash Size in Bits	128 Mega Bits = 07FFFFFh
85h	FFh	Flash Size in Bits	
86h	FFh	Flash Size in Bits	
87h	07h	Flash Size in Bits	
88h	44h	Bit[7:5]=010 8 Mode Bits are needed Bit[4:0]=00100 16 Dummy Bits are needed	Fast Read Quad I/O Setting
89h	EBh	Quad Input Quad Output Fast Read Opcode	
8Ah	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Quad Output Setting
8Bh	6Bh	Single Input Quad Output Fast Read Opcode	
8Ch	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Dual Output Setting
8Dh	3Bh	Single Input Dual Output Fast Read Opcode	
8Eh	80h	Bit[7:5]=100 8 Mode bits are needed Bit[4:0]=00000 No Dummy bits are needed	Fast Read Dual I/O Setting
8Fh	BBh	Dual Input Dual Output Fast Read Opcode	
90h	FEh	Bit[7:5]=111 Reserved Bit[4]=1 support (4-4-4) Fast Read Bit[3:1]=111 Reserved Bit[0]=0 Not support (2-2-2) Fast Read	
91h	FFh	Reserved	
92h	FFh	Reserved	
93h	FFh	Reserved	
94h	FFh	Reserved	
95h	FFh	Reserved	
96h	00h	No Mode Bits or Dummy Bits for (2-2-2) Fast Read	
97h	00h	Not support (2-2-2) Fast Read	
98h	FFh	Reserved	
99h	FFh	Reserved	
9Ah	08h	Bit[7:5]=000 No Mode bits are needed Bit[4:0]=01000 8 Dummy bits are needed	
9Bh	EBh	QPI Fast Read Opcode	
9Ch	0Ch	Sector Type 1 Size (4KB)	Sector Erase Type & Opcode
9Dh	20h	Sector Type 1 Opcode	
9Eh	0Fh	Sector Type 2 Size (32KB)	
9Fh	52h	Sector Type 2 Opcode	
A0h	10h	Sector Type 3 Size (64KB)	Sector Erase Type & Opcode
A1h	D8h	Sector Type 3 Opcode	
A2h	00h	Sector Type 4 Size (256KB) – Not supported	
A3h	00h	Sector Type 4 Opcode – Not supported	
...(1)	FFh	Reserved	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
FFh	FFh	Reserved	

Notes:
1. Data stored in Byte Address 10h to 7Fh & A4h to FFh are Reserved, the value is FFh.
2. 1 Dword = 4 Bytes
3. PID(x) = Parameter Identification Table (x)

10.2.29. Erase Security Sectors (44h)

The FM25Q128 offers two 512-byte Security Sectors which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Sector instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “44h” followed by a 24-bit address A23-A0 to erase one of the two Security Sectors.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector #0 page0	00h	0 0 0 0	0 0 0 0	Don’t Care
Security Sector #0 page1	00h	0 0 0 0	0 0 0 1	Don’t Care
Security Sector #1 page0	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Sector #1 page1	00h	0 0 0 1	0 0 0 1	Don’t Care

The Erase Security Sector instruction sequence is shown in Figure 59. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After CS# is driven high, the self-timed Erase Security Sector operation will commence for a time duration of t_{SE} (See “11.6 AC Electrical Characteristics”). While the Erase Security Sector cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Sector cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

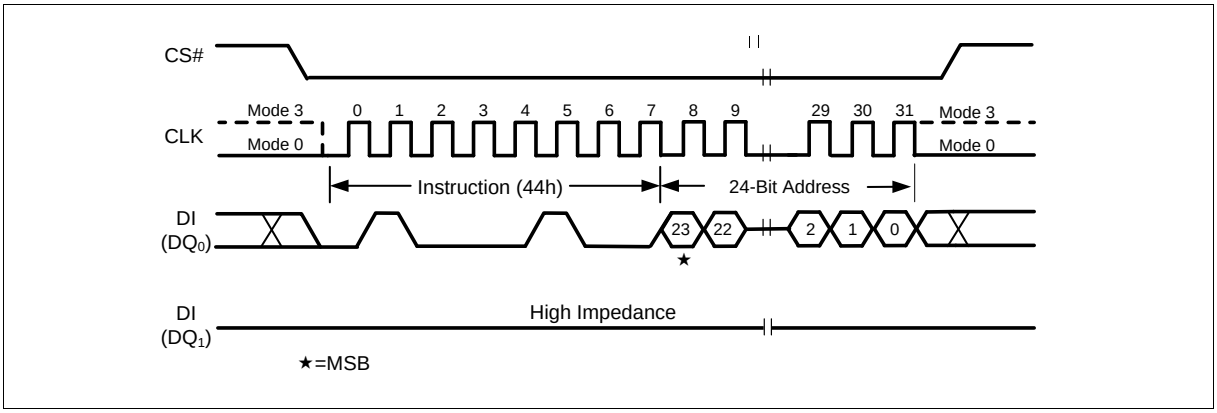


Figure 59 Erase Security Sectors Instruction (SPI Mode only)

10.2.30. Program Security Sectors (42h)

The Program Security Sector instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of Security Sector data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Sector Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “42h” followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector #0 page0	00h	0 0 0 0	0 0 0 0	Don’t Care
Security Sector #0 page1	00h	0 0 0 0	0 0 0 1	Don’t Care
Security Sector #1 page0	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Sector #1 page1	00h	0 0 0 1	0 0 0 1	Don’t Care

The Program Security Sector instruction sequence is shown in Figure 60.

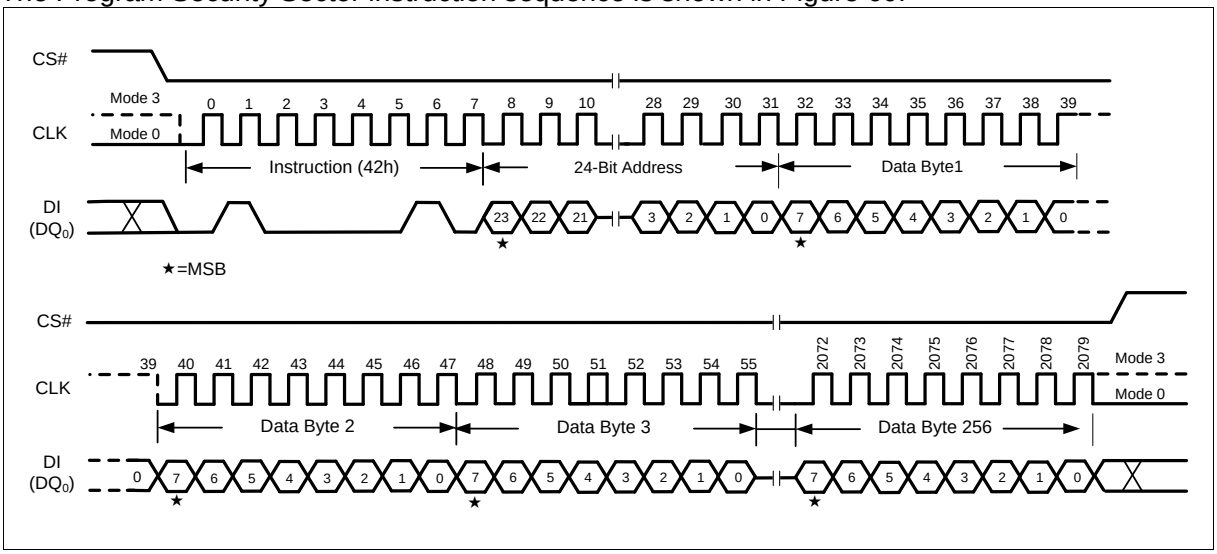


Figure 60 Program Security Sectors Instruction (SPI Mode only)

10.2.31. Read Security Sectors (48h)

The Read Security Sector instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four Security Sectors. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “48h” followed by a 24-bit address A23-A0 and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin.

After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will be reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving CS# high. The Read Security Sector instruction sequence is shown in Figure 61.

If a Read Security Sector instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Security Sector instruction allows clock rates from D.C. to a maximum of FR (see “11.6 AC Electrical Characteristics”).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector #0 page0	00h	0 0 0 0	0 0 0 0	Don’t Care
Security Sector #0 page1	00h	0 0 0 0	0 0 0 1	Don’t Care
Security Sector #1 page0	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Sector #1 page1	00h	0 0 0 1	0 0 0 1	Don’t Care

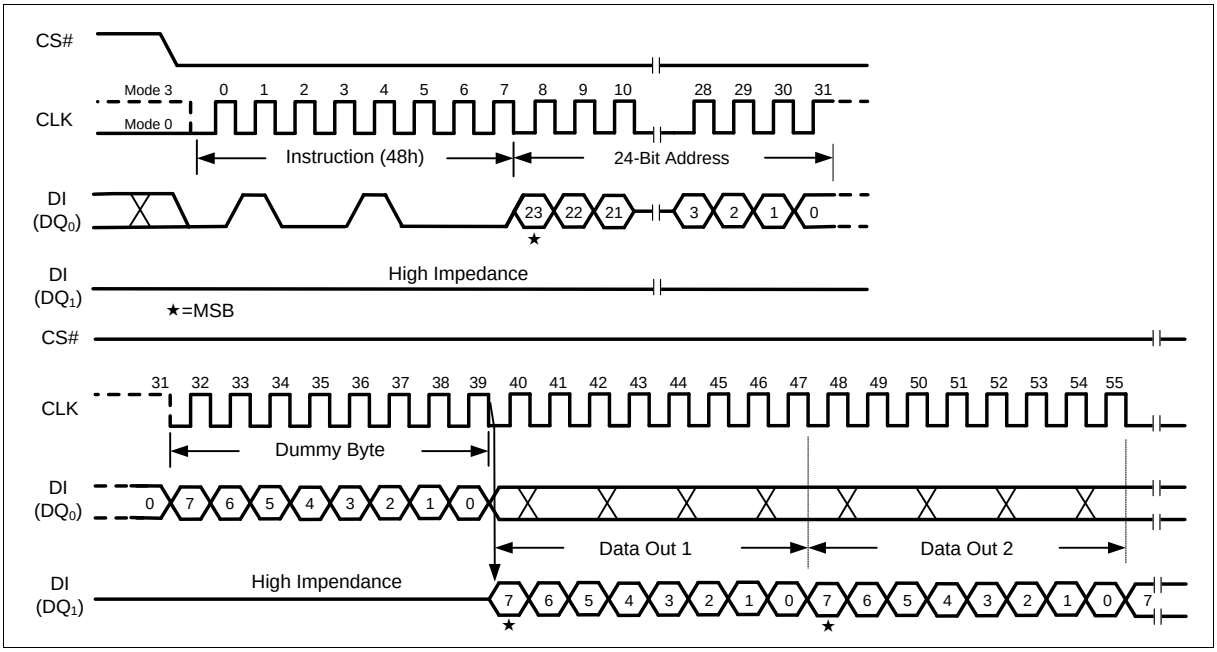


Figure 61 Read Security Sectors Instruction (SPI Mode only)

10.2.32. Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by “Set Burst with Wrap” (77h) command and the number of dummy clocks can be configured by LC[1:0].

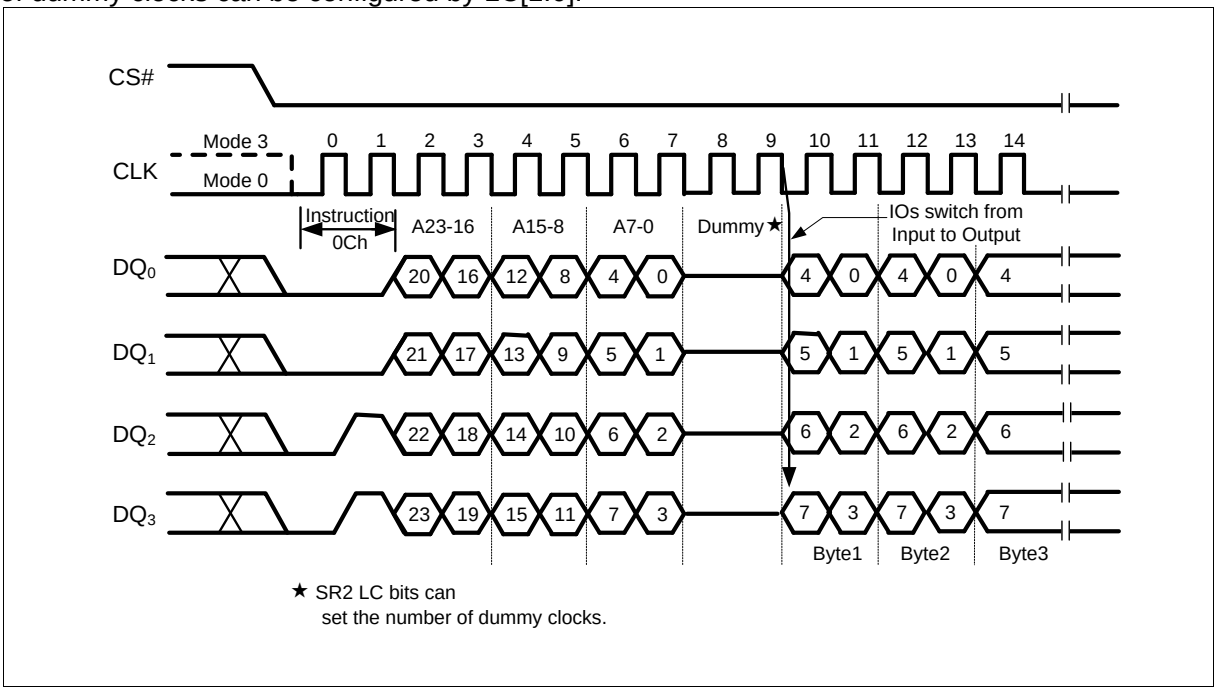


Figure 62 Burst Read with Wrap Instruction (QPI Mode only)

10.2.33. Enable QPI (38h)

The FM25Q128 support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode can not be used at the same time. “Enable QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an “Enable QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enable QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

See “Table 12” for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and the Wrap Length setting will remain unchanged.

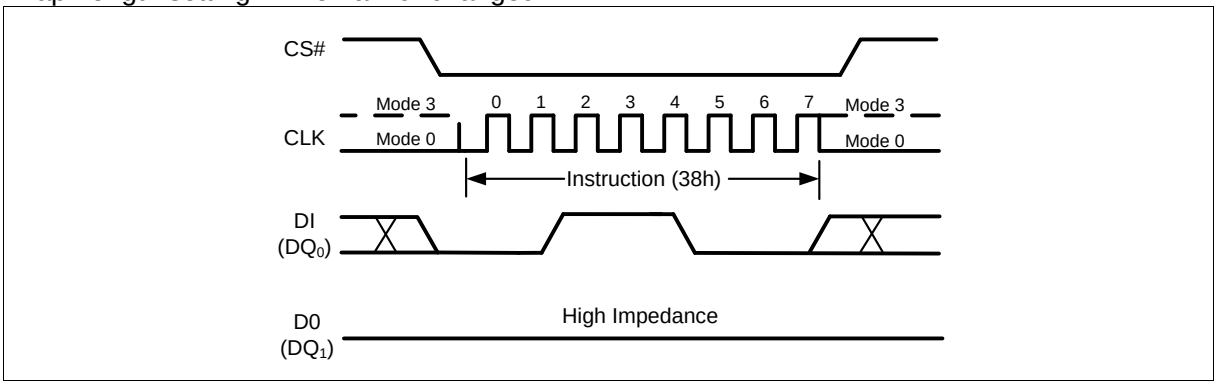


Figure 63 Enable QPI Instruction (SPI Mode only)

10.2.34. Disable QPI (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, a “Disable QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and the Wrap Length setting will remain unchanged.

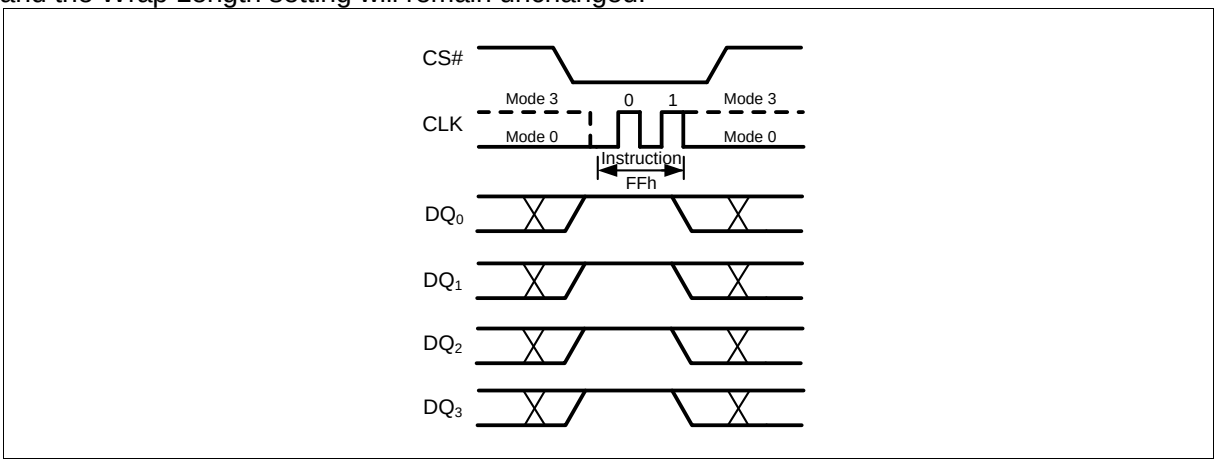


Figure 64 Disable QPI Instruction (QPI Mode only)

10.2.35. Individual Block/Sector Lock (36h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP[2:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset are 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated in Figure 12, an Individual Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

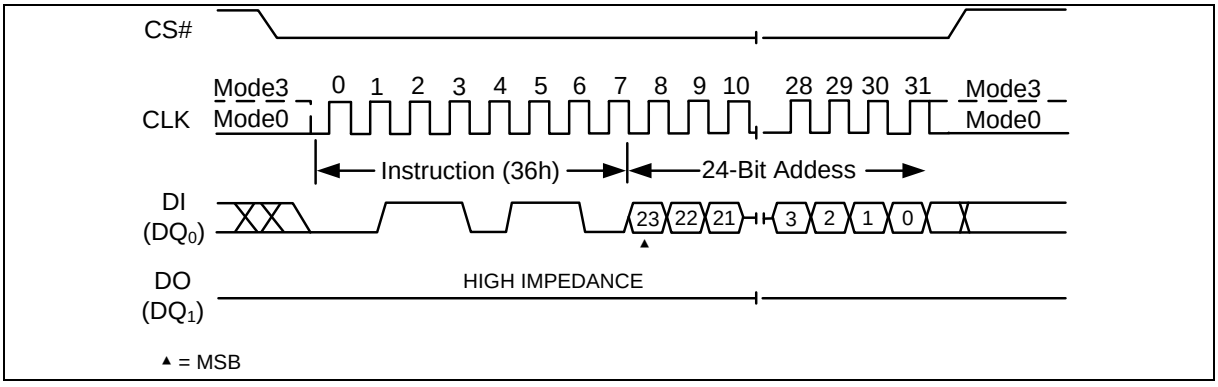


Figure 65 Individual Block/Sector Lock Instruction (SPI)

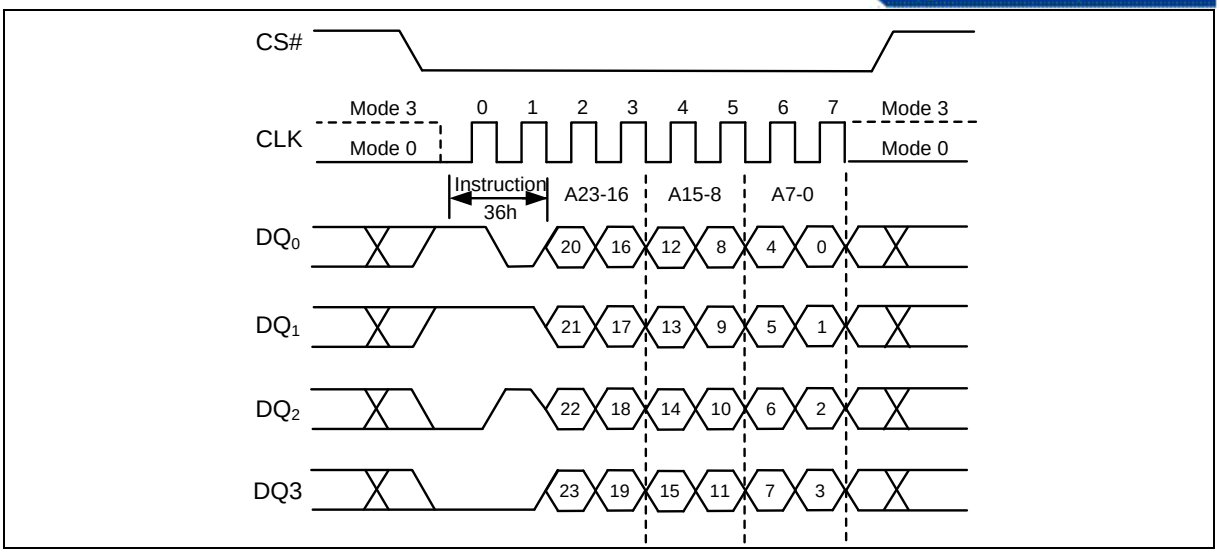


Figure 66 Individual Block/Sector Lock Instruction (QPI Mode)

10.2.36. Individual Block/Sector Unlock (39h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP[2:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset are 1, so the entire memory array is being protected.

To unlock a specific block or sector as illustrated in Figure 12, an Individual Block/Sector Unlock command must be issued by driving CS# low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

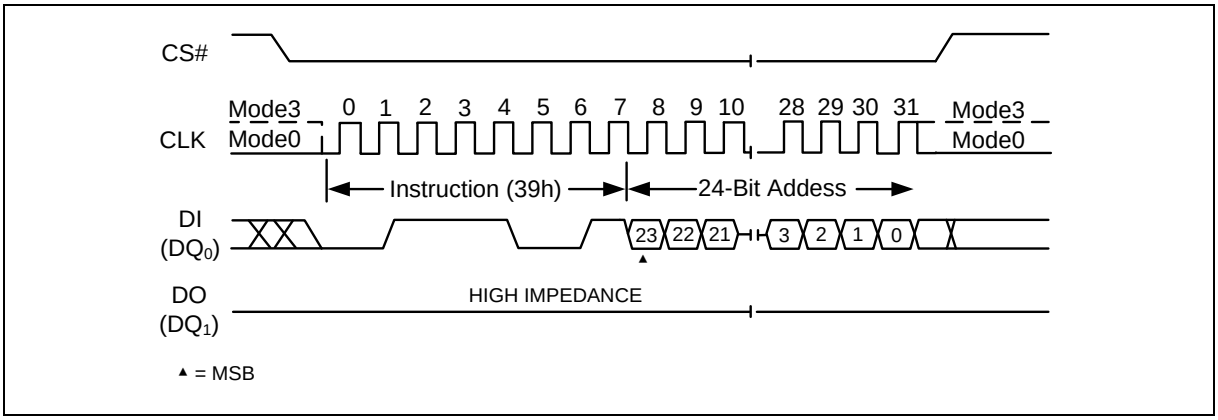


Figure 67 Individual Block/Sector Unlock Instruction (SPI Mode)

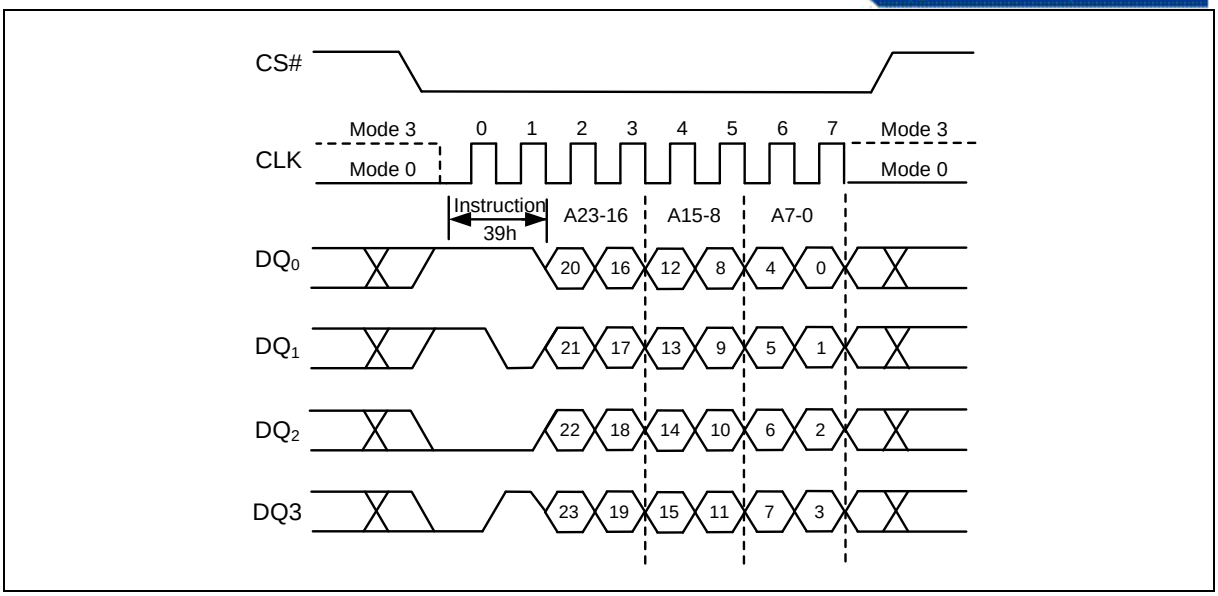


Figure 68 Individual Block/Sector Unlock Instruction (QPI Mode)

10.2.37. Read Block/Sector Lock (3Dh)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, TB, BP[2:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset are 1, so the entire memory array is being protected.

To read out the lock bit of a specific block or sector as illustrated in Figure 12, an Read Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and 8-bit data out, then driving CS# high. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 68. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

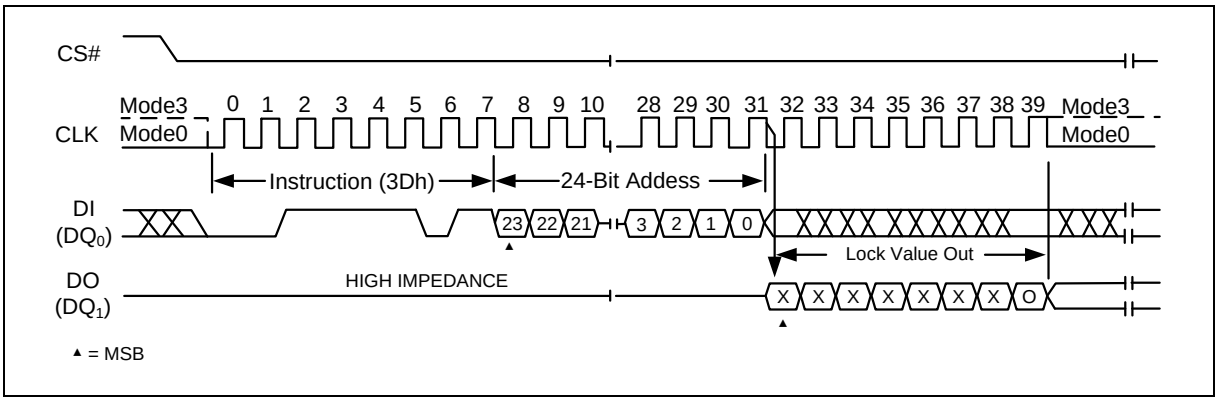


Figure 69 Read Block/Sector Lock Instruction (SPI Mode)

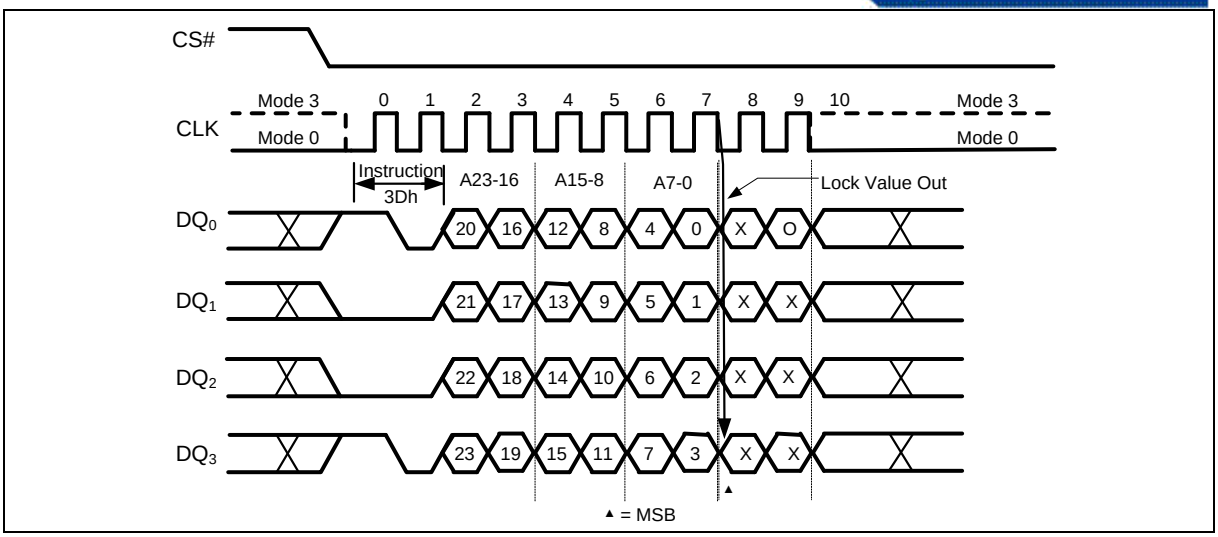


Figure 70 Read Block/Sector Lock Instruction (QPI Mode)

10.2.38. Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving CS# low, shifting the instruction code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

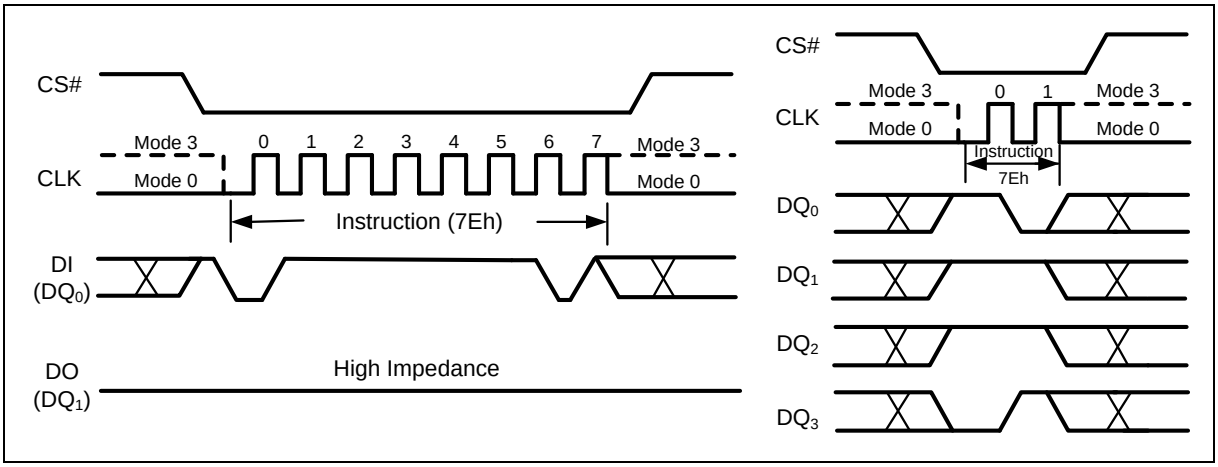


Figure 71 Global Block/Sector Lock Instruction for SPI Mode (left) or QPI Mode (right)

10.2.39. Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving CS# low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

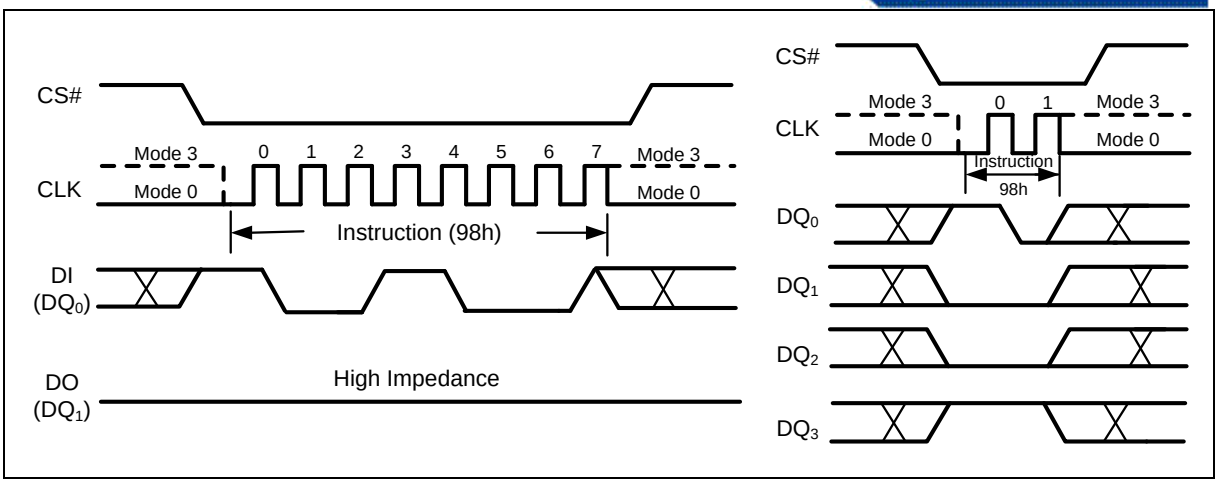


Figure 72 Global Block/Sector Unlock Instruction for SPI Mode (left) or QPI Mode (right)

10.2.40. Enable Reset (66h) and Reset (99h)

Because of the small package and the limitation on the number of pins, the FM25Q128 provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Read parameter setting P7-P0, Continuous Read Mode bit setting M7-M0 and Wrap Bit setting W6-W4.

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately t_{RPH} to reset. During this period, no command will be accepted.

It is recommended that the device exit QPI mode before executing these two commands to initiate a reset.

It is recommended to check the WIP bit in Status Register before issuing the Reset command sequence.

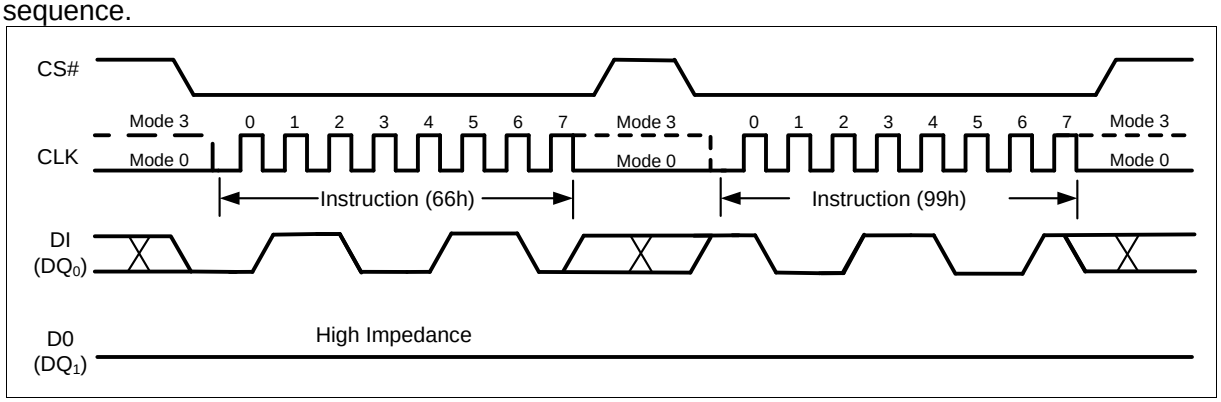


Figure 73 Enable Reset and Reset Instruction Sequence (SPI Mode)

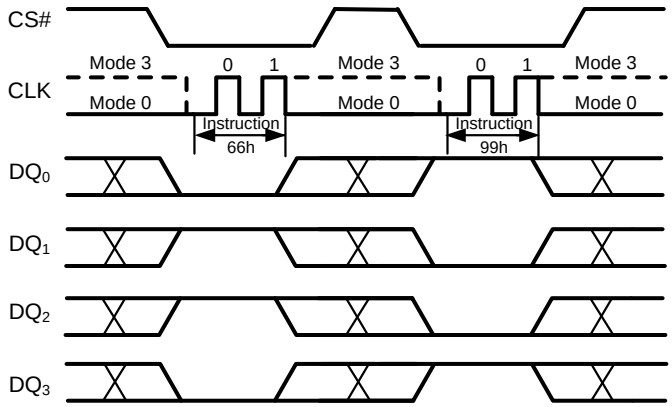


Figure 74 Enable Reset and Reset Instruction Sequence (QPI Mode)

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pin with Respect to Ground	-0.5V to V_{CC}+0.4V
V_{CC}	-0.5V to 4.0V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2. Pin Capacitance

Applicable over recommended operating range from: T_A = 25°C, f = 1 MHz.

Symbol	Test Condition	Max	Units	Conditions
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}(1)	Output Capacitance	8	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

11.3. Power-up and Power-Down Timing

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on VCC) until VCC reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU}
- VSS at power-down

A simple pull-up resistor (generally of the order of 100 kΩ) on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} has elapsed after the moment that VCC rises above the minimum VCC threshold. See Figure 75. However, correct operation of the device is not guaranteed if VCC returns below VCC (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

After power-up (t_{PU}), the device is in Standby mode (not Deep Power Down mode), draws CMOS standby current (I_{CC1}), and the WEL bit is reset.

Power-down or voltage drops below VCC (low) for a period of t_{PD} for the part to initialize correctly on power-up. See Figure 76. In the event Power-on Reset (POR) did not complete correctly after power up, or receiving a software reset command (RESET) will restart the POR process.

Normal precautions must be taken for supply rail decoupling to stabilize the VCC supply at the device. Each device in a system should have the VCC rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1 µf).

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
t_{PU} (1)	$V_{CC,min}$ to read		35	μs
t_{PD} (1)	V_{CC}(low) time	1.0		μs
V_{CC}(low) (1)	V_{CC}(low voltage for initialization to occur when WIP=0)	1.0		V
	V_{CC}(low voltage for initialization to occur when WIP=1)	2.3		

Note: 1. This parameter is characterized and is not 100% tested.

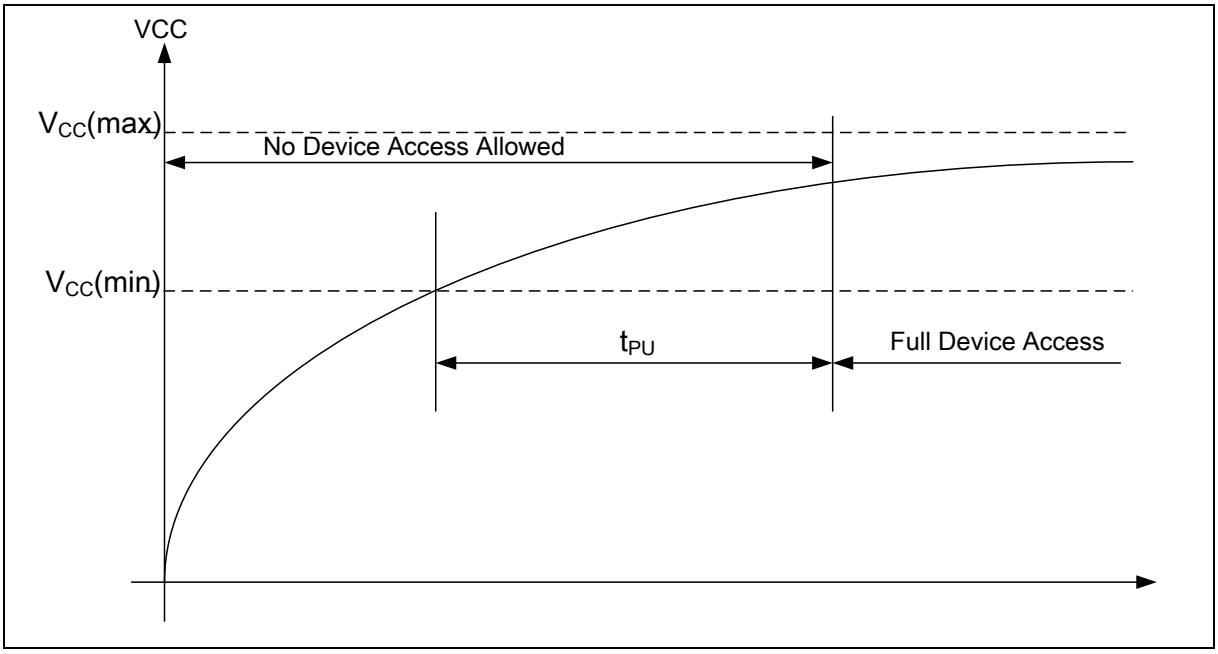


Figure 75 Power-up Timing

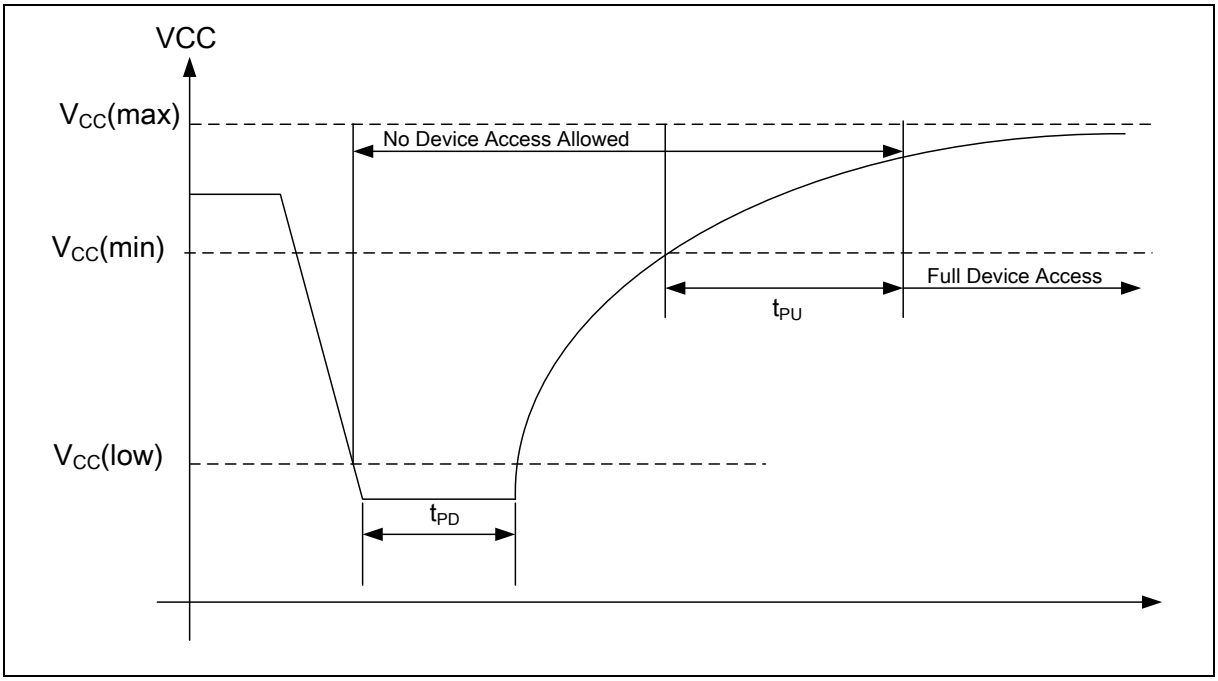


Figure 76 Power-down and Voltage Drop

11.4. DC Electrical Characteristics

Table 13 DC Characteristics

Applicable over recommended operating range from: T_A = -40 ℃ to 85 ℃, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Vcc	Supply Voltage		2.7		3.6	V
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	V_{CC}=3.6V, CS# = V_{CC}, V_{IN} = Vss or V_{CC}		1	5	μA
I_{CC2}	Deep Power-down Current			1	5	μA
I_{CC3}	Current Read Data / Dual / Quad 1MHz(1)	V_{CC}=3.6V CLK=0.1V_{CC}/0.9V_{CC} DQ open			15	mA
I_{CC3}	Current Read Data / Dual / Quad 50MHz(1)				20	mA
I_{CC3}	Current Read Data / Dual / Quad 80MHz(1)				30	mA
I_{CC3}	Current Read Data / Dual / Quad 104MHz(1)				40	mA
I_{CC4}	Operating Current (WRSR)	V_{CC}=3.6V,CS#=V_{CC}		8	12	mA
I_{CC5}	Operating Current (PP)			20	25	mA
I_{CC6}	Operating Current (SE)			20	25	mA
I_{CC7}	Operating Current (BE)			20	25	mA
V_{IL}(2)	Input Low Voltage		-0.5		0.3V_{CC}	V
V_{IH}(2)	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 μA	V_{CC}-0.2			V

Notes:

1. Checker Board Pattern.
2. V_{IL} min and V_{IH} max are reference only and are not tested.

11.5. AC Measurement Conditions

Table 14 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		20	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

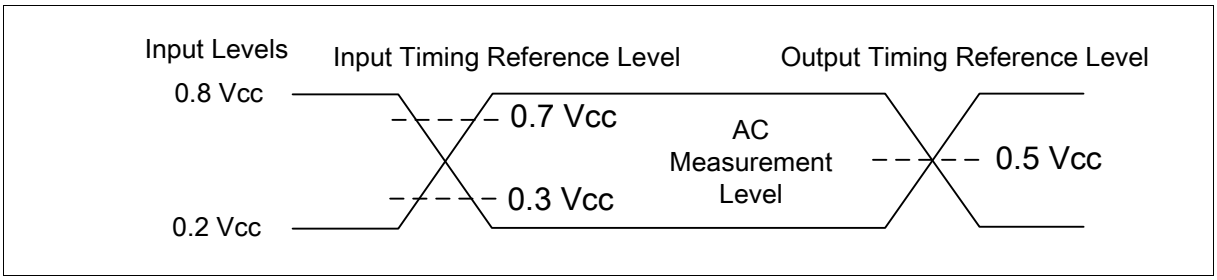


Figure 77 AC Measurement I/O Waveform

11.6. AC Electrical Characteristics

Table 15 AC Characteristics

Applicable over recommended operating range from: T_A = -40℃ to 85℃, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_R	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR			104	MHz
f_R	Serial Clock Frequency for READ, RDSR, RDID			50	MHz
t_{CH1}(1)	Serial Clock High Time	4.5			ns
t_{CL1}(1)	Serial Clock Low Time	4.5			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL1}	CS# High Time (for Array Read → Array Read)	10			ns
t_{SHSL2}	CS# High Time (for Erase or Program → Read Status Registers) Volatile Status Register Write Time	50			ns
t_{SHQZ}(2)	Output Disable Time			7	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			12	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			8	ns
t_{CLQV}	Output Valid from CLK			7	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time after CS# High	100			ns
t_{DP}(2)	CS# High to Deep Power-down Mode			3	µs
t_{RES1}(2)	CS# High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2}(2)	CS# High to Standby Mode with Electronic Signature Read			1.8	µs
t_W	Write Status Register Cycle Time		10	15	ms
t_{PP}	Page Programming Time		0.35	2	ms
t_{SE}	Sector Erase Time		90	300	ms
t_{BE}	Block Erase Time (32KB)		150	1500	ms
t_{BE}	Block Erase Time (64KB)		250	2000	ms
t_{CE}	Chip Erase Time		50	320	s
t_{RS}	Reset set time	15			ns
t_{RLRH}	Reset pulse width	2			us
t_{RHSL}	Reset Recorvery time(not for program or erase operation)	50			us
	Reset Recorvery time(for WRSR operation)	20			ms
	Reset Recorvery time(for PP operation)	20			us
	Reset Recorvery time(for SE operation)	20			ms
	Reset Recorvery time(for BE operation)	40			ms
	Reset Recorvery time(for CE operation)	100			ms

Notes:

1. $T_{CH1}+T_{CL1} >= 1 / F_{CLK}$;
2. This parameter is characterized and is not 100% tested.

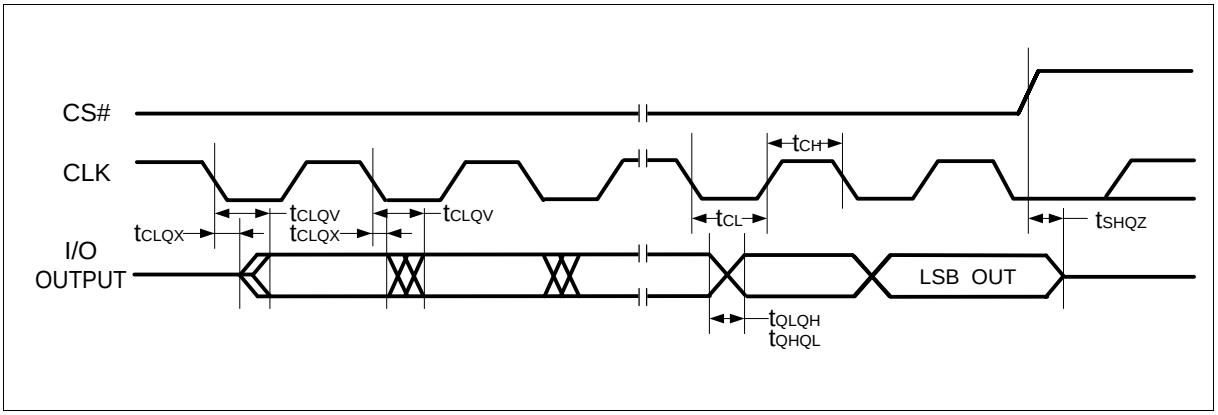


Figure 78 Serial Output Timing

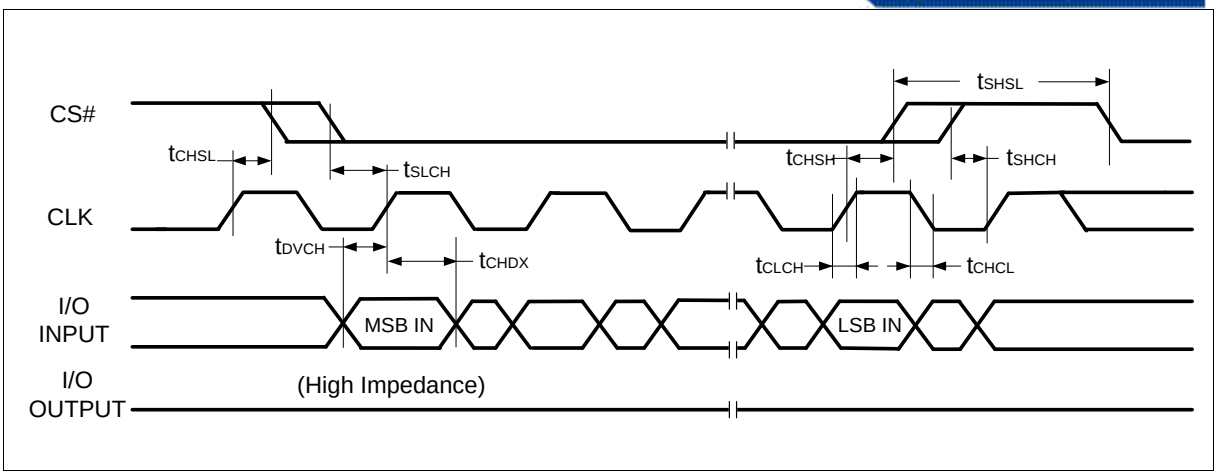


Figure 79 Serial Input Timing

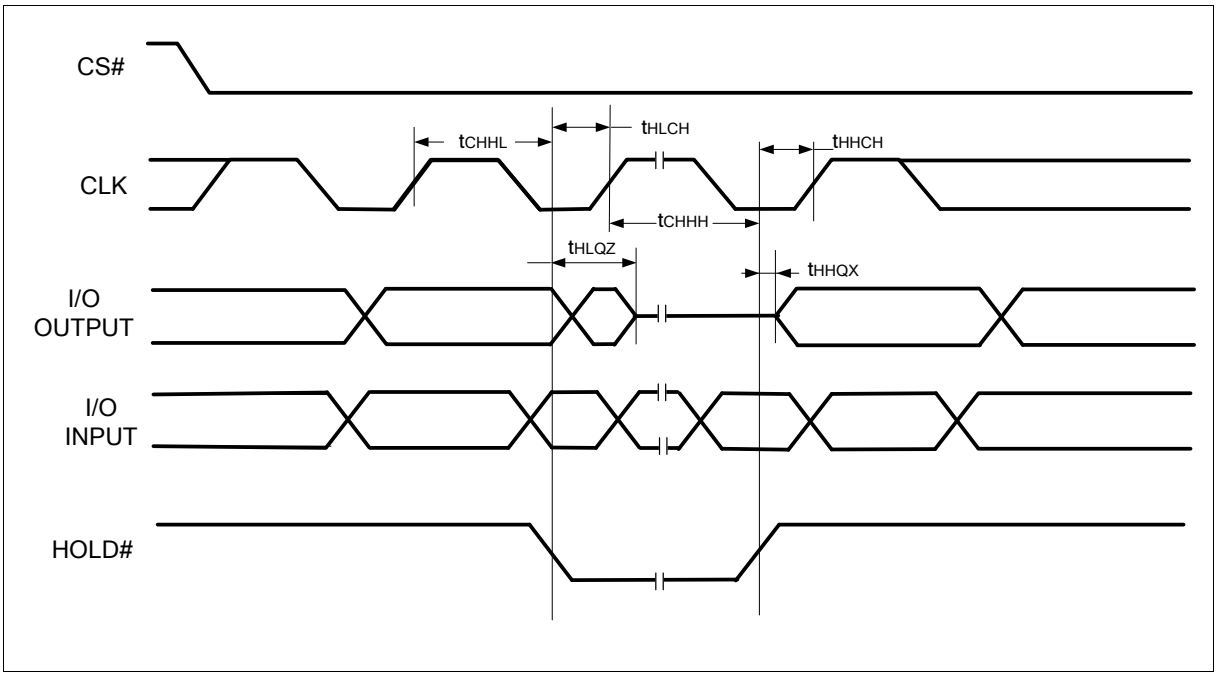


Figure 80 Hold Timing

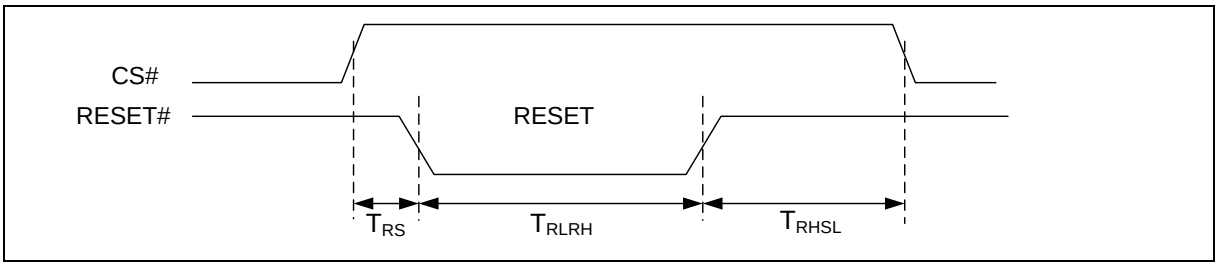


Figure 81 RESET Timing

12. Ordering Information

FM 25Q 128 -XXX -C -H

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

25Q = 2.7~3.6V Serial Flash with 4KB Uniform-Sector,
Dual/Quad SPI & QPI

Product Density

128 = 128M-bit

Package Type

SOB = 8-pin SOP (208mil）
DND = 8-pin TDFN (8x6mm)
DNA = 8-pin TDFN (5x6mm)

Product Carrier

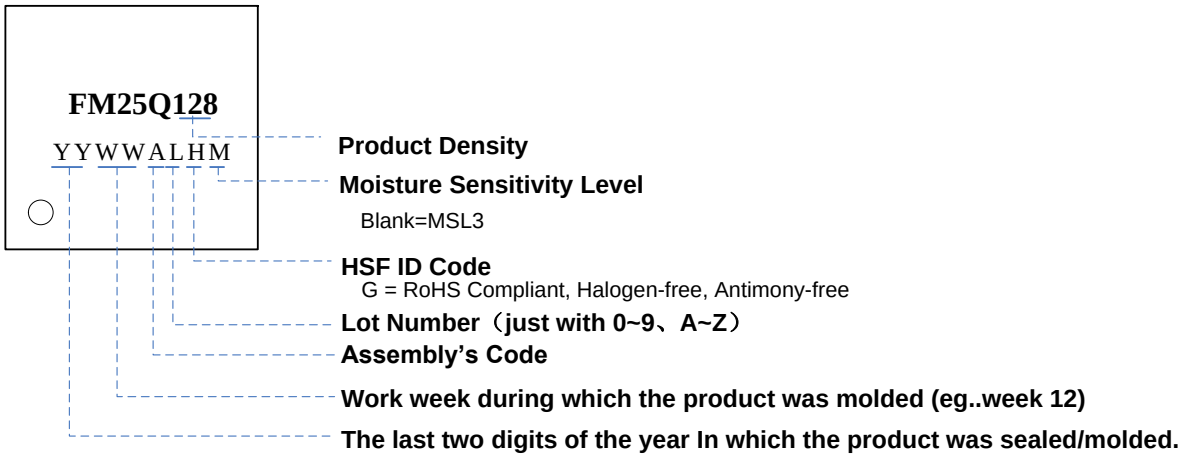
U = Tube
T = Tape and Reel
A = Trap

HSF ID Code

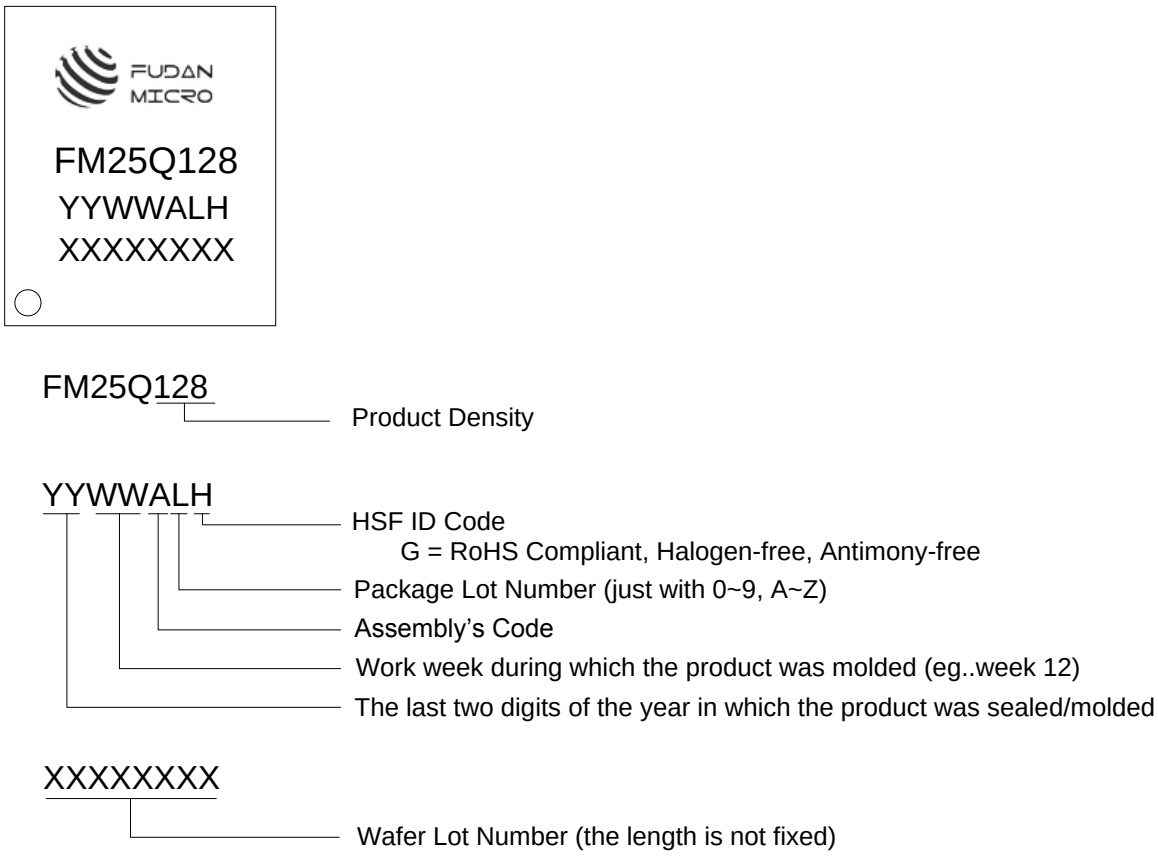
G = RoHS Compliant, Halogen-free, Antimony-free

13. Part Marking Scheme

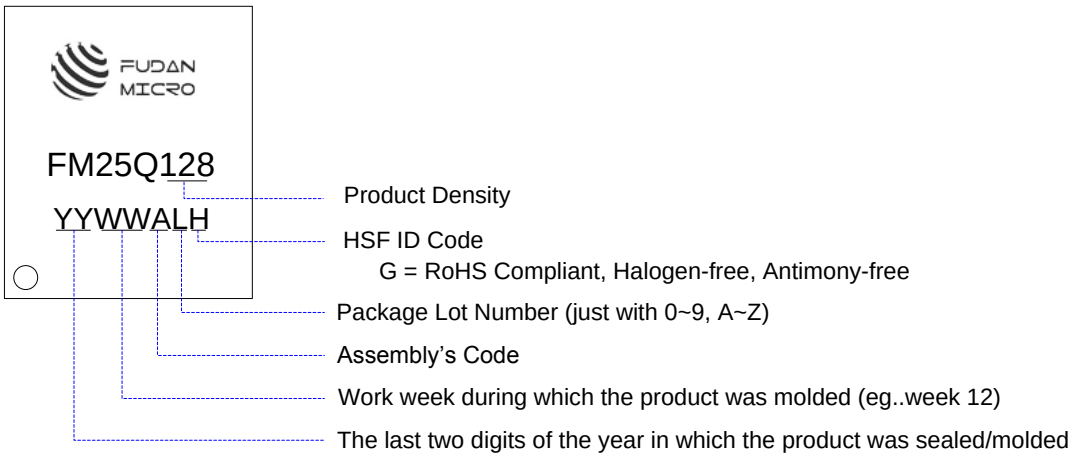
13.1. SOP8 (208mil)



13.2. TDFN8 (8x6mm)



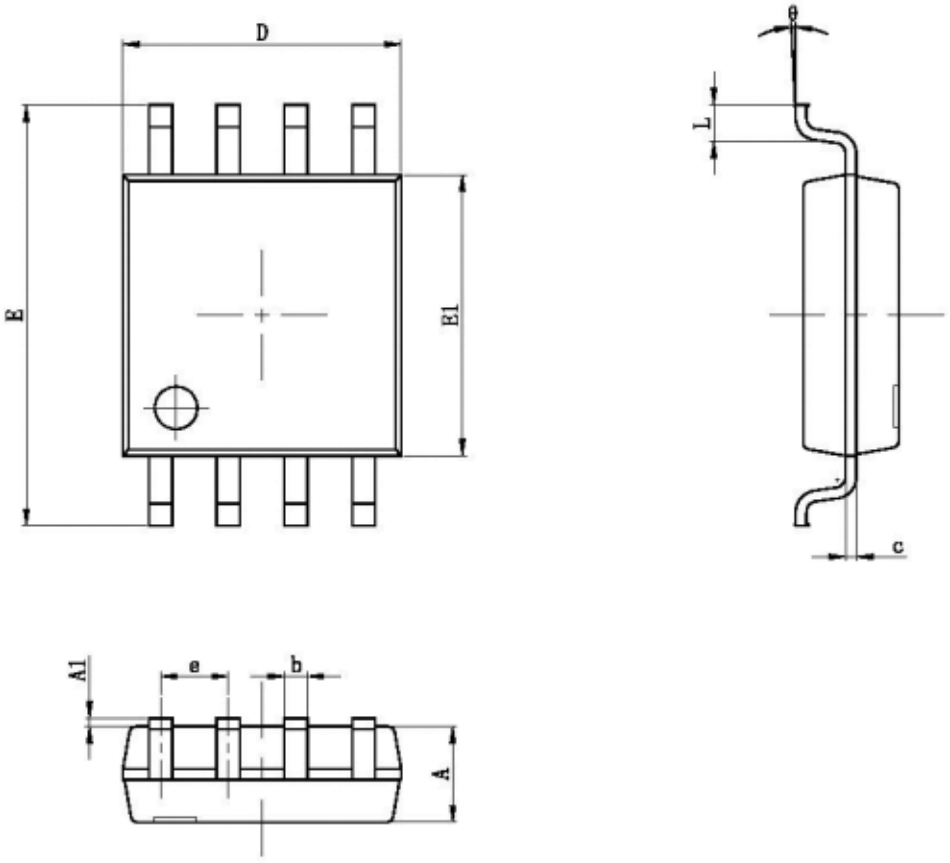
13.3. TDFN8 (5x6mm)



14. Packaging Information

14.1. SOP8 (208mil)

SOP 8 (208mil)



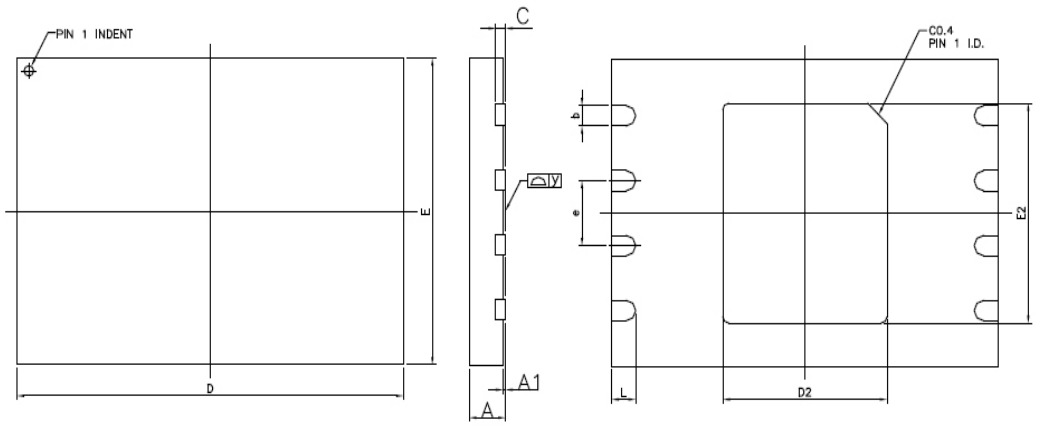
Symbol	MIN	MAX
A	– –	2.100
A1	0.050	0.250
b	0.350	0.500
c	0.100	0.250
D	5.130	5.330
E1	5.180	5.380
E	7.700	8.100
e	1.270(BSC)	
L	0.500	0.850
θ	0°	8°

NOTE:

1. **Dimensions are in Millimeters.**

14.2. TDFN8 (8x6mm)

TDFN8 (8x6mm)

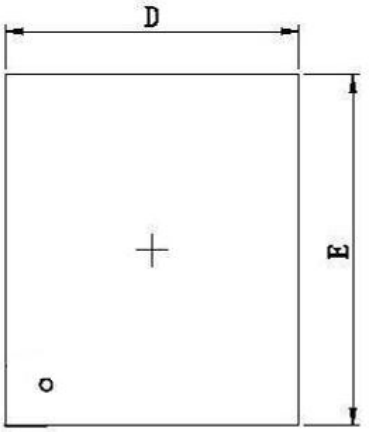


Symbol	MIN	MAX
e	1.270 B C	
D	7.900	8.100
E	5.900	6.100
L	0.450	0. 0
A	0.700	0.800
A1	0.000	0.050
C	0.180	0.250
b	0.350	0.450
D2	3.300	3.500
E2	4.200	4.400

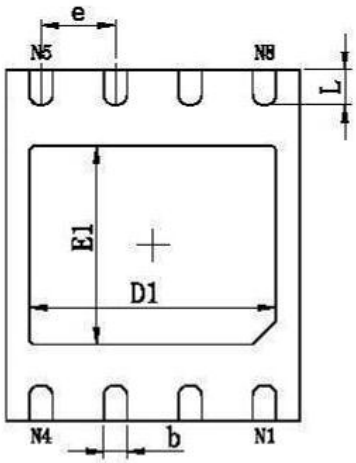
Note:
1. Dimensions are in Millimeters.

14.3. TDFN8 (5x6mm)

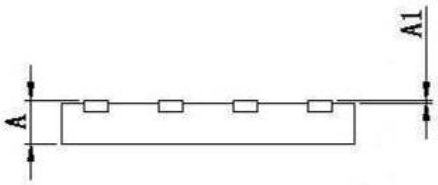
TDFN8 (5x6mm)



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D	4.900	5.100
E1	3.300	3.500
D1	4.100	4.300
E	5.900	6.100
b	0.350	0.450
e	1.270TYP	
L	0.524	0.676

NOTE:

1. **Dimensions are in Millimeters.**

15. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
preliminary	Nov. 2017	75		Initial Document Release.
1.0	Aug. 2018	77		1. Update AC Characteristics 2. Added the TDFN8 (5X6mm) offering and parts.
1.1	May. 2019	77		Update description for HOLD# pin as RESET#

Sales and Service

Shanghai Fudan Microelectronics Group Co., Ltd.
Address: Bldg No. 4, 127 Guotai Rd,
Shanghai City China.
Postcode: 200433
Tel: (86-021) 6565 5050
Fax: (86-021) 6565 9115

Shanghai Fudan Microelectronics (HK) Co., Ltd.
Address: Unit 506, 5/F., East Ocean Centre, 98 Granville Road, Tsimshatsui East, Kowloon, Hong Kong
Tel: (852) 2116 3288 2116 3338
Fax: (852) 2116 0882

Beijing Office
Address: Room 423, Bldg B, Gehua Building,
1 QingLong Hutong, Dongzhimen Alley north Street,
Dongcheng District, Beijing City, China.
Postcode: 100007
Tel: (86-010) 8418 6608
Fax: (86-010) 8418 6211

Shenzhen Office
Address: Room.1301, Century Bldg, No. 4002, Shengtingyuan Hotel, Huaqiang Rd (North),
Shenzhen City, China.
Postcode: 518028
Tel: (86-0755) 8335 0911 8335 1011 8335 2011 8335 0611
Fax: (86-0755) 8335 9011

Shanghai Fudan Microelectronics (HK) Ltd Taiwan Representative Office
Address: Unit 1225, 12F., No 252, Sec.1 Neihu Rd., Neihu Dist., Taipei City 114, Taiwan
Tel : (886-2) 7721 1889 (886-2) 7721 1890
Fax: (886-2) 7722 3888

Shanghai Fudan Microelectronics (HK) Ltd Singapore Branch Office
Address: 47 Kallang Pudding Road, #08-06
The Crescent @ Kallang, Singapore 349318
Tel: +65 64430860
Fax: +65 64431215
Email: kttan@fmsh.com

Fudan Microelectronics (USA) Inc.
Address: 97 E Brokaw Road, Suite 320,San Jose,CA 95112
Tel: (+1)408-335-6936
Contact name: Xinyue Huang
Email: fmus@fmsh.com

Web Site: http://www.fmsh.com/